PY32T020 Datasheet

32-bit ARM® Cortex®-M0+ Microcontroller

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Puya Semiconductor (Shanghai) Co., Ltd.

PY32T020 Series

32-bit ARM® Cortex®-M0+ Microcontroller

Features

- Core
  - — ARM® 32-bit Cortex®-M0+ CPU
  - — Frequency up to 48 MHz
- Memories
  - — Maximum 32 KB Flash memory
  - — Maximum 4 KB SRAM
- Clock management
  - — 24/48 MHz High-speed internal RC oscillator (HSI)
  - — 32.768 kHz Low-speed internal RC oscillator (LSI)
  - — 4 - 8 MHz High-speed external crystal oscillator (HSE)
  - — 32.768 kHz Low-speed external crystal oscillator (LSE)
  - — External clock input
- Power management and reset
  - — Operating voltage: 1.8 - 5.5 V
  - — Low power modes: Sleep/Stop/Deep_stop/Hibernate
  - — Power-on/power-down reset (POR/PDR)
  - — Brown-out reset (BOR)
- General-purpose input and output (I/O)
  - — Up to 26 I/Os, all available as external interrupts
  - — 5 GPIOs supporting high sink current (configurable as 80mA/60mA/40mA/20mA) for driving common-cathode LED digital tubes
  - — 8 GPIOs as LED SEG with constant-current drive
  - — All GPIOs can serve as LCD COM with 1/2 Bias
- Touch Key
  - —High-sensitivity for non-contact touch
  - —10 V dynamic CS test-passed anti-interference mode
  - —26 touch channels with derived functions
  - —Low-power touch mode with multi-touch wake-up capability (<8 μA system current consumption)
- 1 x 12-bit ADC
  - — Up to 10 external channels and 3 internal channels
  - — Voltage reference options: embedded 0.6V/1.5 V/2.048 V/2.5 V and V_{CC}
- Timers
  - — 1 x 16-bit advanced-control timer (TIM1)
  - — 1 x 16-bit general-purpose timer (TIM14)
  - — 1 x independent watchdog timer (IWDG)
  - — 1 x SysTick timer
- RTC
- Communication interfaces
  - — 1 x serial peripheral interface (SPI)
  - — 3 x universal asynchronous receiver transmitters (UARTs)
  - — 1 x I^2C interface, supporting Standard mode (100 kHz), Fast mode (400 kHz) and Fast mode plus (1 MHz)
- Hardware CRC-32 module
- 2 x comparators
- Unique UID
- Serial wire debug (SWD)
- Operating temperature - 40 - 105 °C
- Packages: QFN28, TSSOP28, SOP28, SOP20, SOP16 and SOP8

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1. Introduction

PY32T020 Series are based on a 32-bit ARM® Cortex®-M0+ core and operates at up to 48 MHz with a wide voltage range. It integrates up to 32 KB Flash and 4 KB SRAM, available in multiple package options. The device integrates I2C, SPI, UART and other communication peripherals. It has one 12-bit ADC, two 16-bit timers, two comparators and 26-channel low-power dual-mode capacitive touch circuit (in Stop mode).

The PY32T020 microcontrollers operate across a temperature range of -40 to 105 °C and a standard voltage range of 1.8 - 5.5 V, providing Sleep/Stop/Deep_stop/Hibernate low-power operating modes for different low-power applications.

The PY32T020 series feature excellent touch button characteristics. Coupled with its outstanding anti-interference performance, it can be adapted in various solutions. Its applications span smart appliances, controllers, handheld equipment, PC peripherals, gaming/GPS platforms, and industrial systems.

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Table 1-1 PY32T020 QFN28 / TSSOP28 / SOP28 series product features and peripheral counts

Peripherals		PY32T020G16U7	PY32T020G16P7	PY32T020G15P7	PY32T020G16S7	PY32T020G15S7	PY32T020G26S7	PY32T020G25S7	PY32T020G36S7	PY32T020G35S7
Flash (KB)		32	32	20	32	20	32	20	32	20
SRAM (KB)		4	4	2	4	2	4	2	4	2
Timers	Advanced control	1								
	General purpose	1								
	SysTick	1								
	Watchdog	1								
Comm. interfaces	SPI	1								
	I^2C	1								
	UART	3								
RTC		Yes								
GPIOs		26	26	26	26	26	26	26	26	26
Touch CH		26	26	26	26	26	26	26	26	26
ADC (external + internal)		10+3	10+3	10+3	10+3	10+3	10+3	10+3	10+3	10+3
LED COM		5	5	5	5	5	5	5	5	5
LED SEG		8	8	8	8	8	8	8	8	8
LCD COM		26								
Comparators		2								
Max. CPU frequency(1)		48 MHz	48 MHz	24 MHz	48 MHz	24 MHz	48 MHz	24 MHz	48 MHz	24 MHz
Operating voltage		1.8 - 5.5 V								
Operating temperature		-40 - 105 ℃								
Packages		QFN28			TSSOP28			SOP28		

1. Products with 20 KB Flash support up to 24 MHz CPU frequency.

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表 1-2 PY32T020 SOP20 / SOP16 / SOP8 series product features and peripheral counts

Peripherals		PY32T020F26S7	PY32T020F25S7	PY32T020W16S7	PY32T020W15S7	PY32T020L15S7
Flash (KB)		32	20	32	20	20
SRAM (KB)		4	2	4	2	2
Timers	Advanced control	1				
	General purpose	1				
	SysTick	1				
	Watchdog	1				
Comm. interfaces	SPI	1				
	I^2C	1				
	UART	3				
RTC		Yes				
GPIOs		18	18	14	14	6
Touch CH		18	18	14	14	6
ADC (external + internal)		10+3	10+3	5+3	5+3	3+3
LED COM		5	5	4	4	-
LED SEG		5	5	4	4	-
LCD COM		18	18	14	14	6
Comparators		2				1
Max. CPU frequency(1)		48 MHz	24 MHz	48 MHz	24 MHz	24 MHz
Operating voltage		1.8 - 5.5 V				
Operating temperature		-40 - 105 ℃				
Packages		SOP20		SOP16		SOP8

1. Products with 20 KB Flash support up to 24 MHz CPU frequency.

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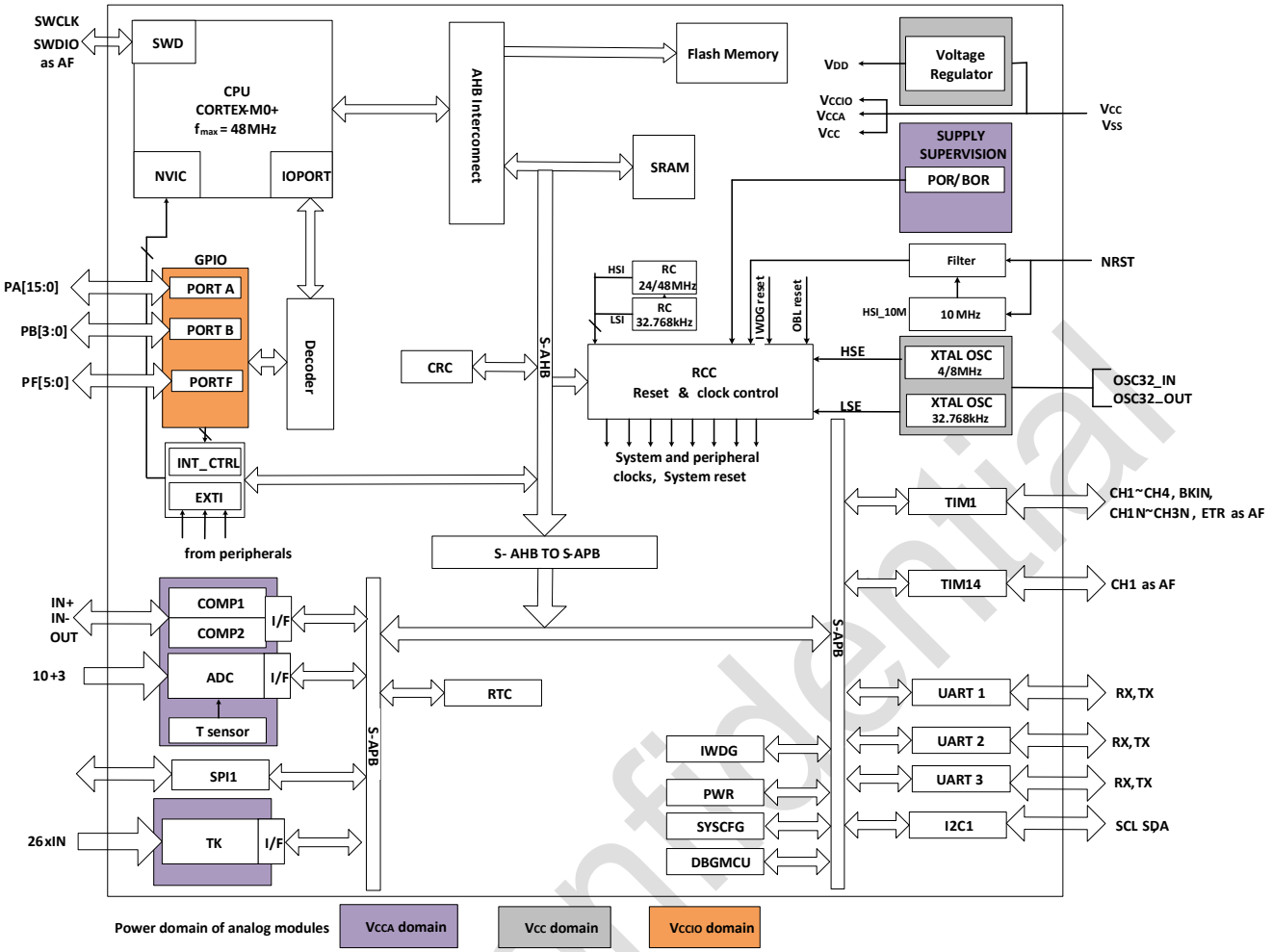

Figure 1-1 System block diagram

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2. Functional overview

2.1. Arm® Cortex®-M0+ core

The Arm® Cortex®- M0+ is an entry-level Arm 32-bit Cortex processor designed for embedded systems. It provides developers with significant benefits, including:

- Simple architecture for easy learning and programming
- Ultra-low power consumption for energy-efficient operation
- Reduced code density

The Arm® Cortex-M0+ processor is a 32-bit core optimized for area and power consumption and is a 2-stage pipeline Von Neumann architecture. The processor offers high-end processing hardware, including single-cycle multipliers, through a streamlined but powerful instruction set and an extensively optimized design. Moreover, it delivers the superior performance expected from a 32-bit architecture computer, with a higher coding density than other 8 and 16-bit microcontrollers.

The Cortex-M0+ is tightly coupled with a Nested Vectored Interrupt Controller (NVIC).

2.2. Memories

Embedded SRAM is accessed by byte (8 bits), half-word (16 bits) or word (32 bits).

The Flash memory is composed of two distinct physical areas:

- The Main flash area consists of application and user data, with up to 4 KB configurable as a User bootloader through customer settings.
- 768 Bytes of Information area:
  - Option bytes
  - UID bytes
  - Factory configuration bytes
  - USER OTP memory

The protection of Main flash area includes the following mechanisms:

- Read protection (RDP) blocks external access
- Write protection (WRP) prevents unintended writes (caused by confusion of program). The minimum protection unit for write protection is 4 KB
- Option byte write protection is a special design for unlock
- SDK protection

2.3. Boot modes

At startup, the nBOOT0 pin and nBOOT1 (stored in option bytes) are used to select one of the three boot options in the following table:

Table 2-1 Boot configuration

Boot modes		Mode	
nBOOT1 bit	**nBOOT0 bit**	**Boot memory size == 0**	**Boot memory size != 0**
X	0	Boot from Main flash	Boot from Main flash

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Boot modes		Mode	
nBOOT1 bit	**nBOOT0 bit**	**Boot memory size == 0**	**Boot memory size != 0**
0	1	Boot from SRAM	Boot from SRAM
1	1	N/A	Boot from Load Flash(1)

1. Products with 20 KB Flash cannot boot from Load Flash.

2.4. Clock management

System clock selection is performed on startup, however the internal RC 24 MHz oscillator is selected as default CPU clock on reset. After the program is operating the system clock frequency and system clock source can be reconfigured. The frequency clocks that can be selected are:

- 24/48 MHz internal high precision HSI clock
- A 32.768 kHz configurable internal LSI clock
- A 4 to 8 MHz HSE clock, and used to enable the CSS function to detect HSE. If CSS fails, the hardware will automatically convert the system clock to HSI, and software configures the HSI frequency. Simultaneously, CPU NMI interrupt is generated.
- A 32.768 kHz LSE clock.

The AHB clock can be divided based on the system clock, and the APB clock can be divided based on the AHB clock. The maximum frequency of the AHB and the APB domains is 48 MHz.

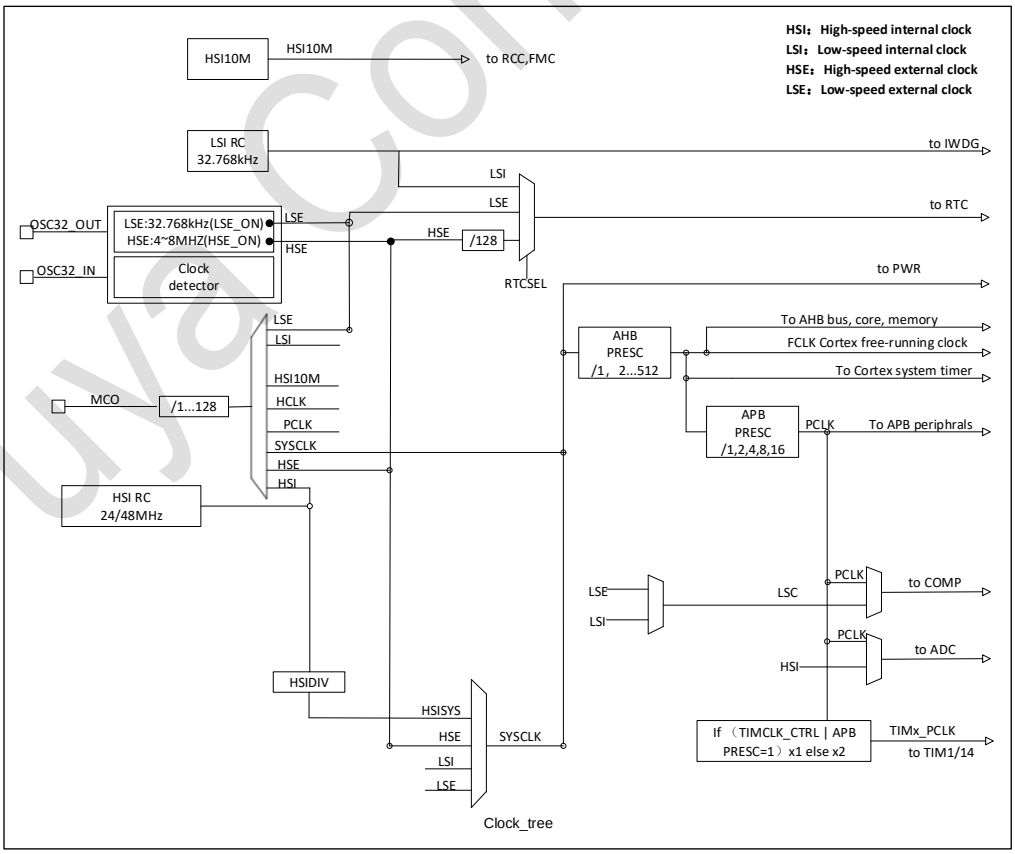

Figure 2-1 System clock structure diagram

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2.5. Power management

2.5.1. Power block diagram

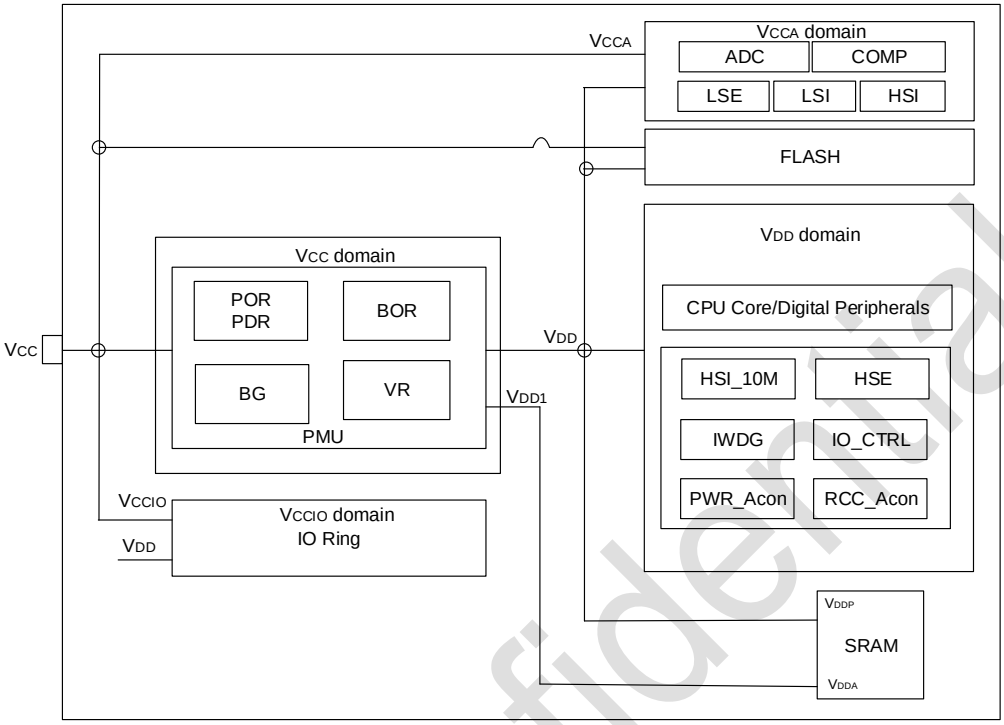

Figure 2-2 Power block diagram

Table 2-2 Power block diagram

No.	Power supply	Power value	Descriptions
1	V_{CC}	1.8 - 5.5 V	The power is supplied to the device through the power pins, with the power supply module comprising: Partial analog circuits
2	V_{CCA}	1.8 - 5.5 V	Powers for most analog modules, sourced from the V_{CC} PAD (a dedicated power PAD can also be designed separately).
3	V_{CCIO}	1.8 - 5.5 V	Power to IO from V_{CC} PAD

2.5.2. Power monitoring

2.5.2.1. Power on reset (POR/PDR)

The Power-on reset (POR) and Power-down reset (PDR) module is designed to provide power-on and power-off reset for the device. The module functions reliably in all modes.

2.5.2.2. Brown-out reset (BOR)

In addition to POR/ PDR, BOR (Brown-out reset) is also implemented. BOR can only be enabled and disabled through the option byte.

When the BOR is turned on, the BOR threshold can be selected by the option byte and both the rising and falling detection points can be individually configured.

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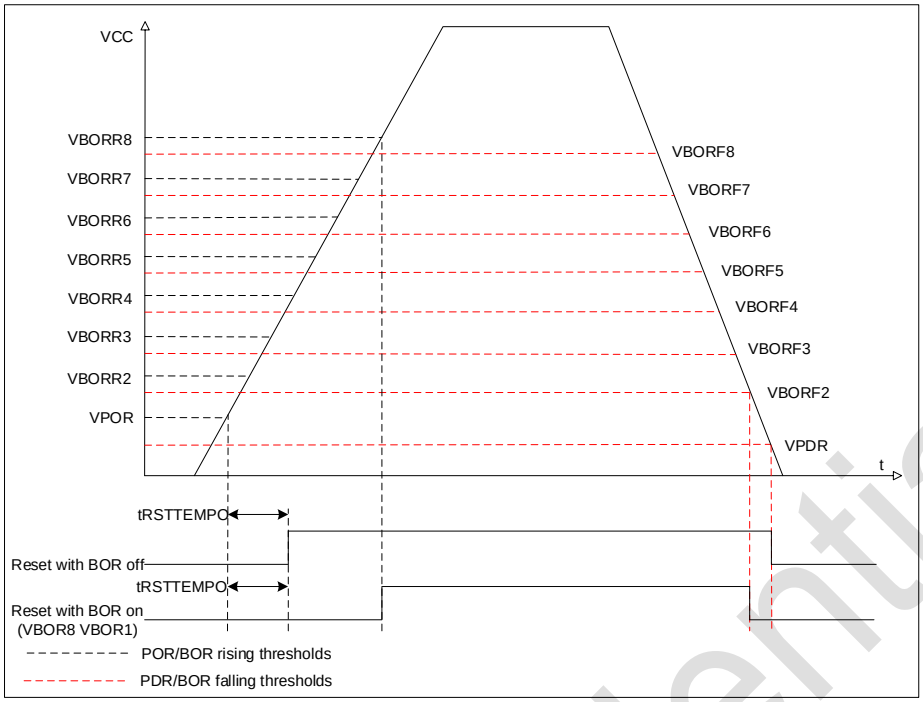

Figure 2-3 POR/PDR/BOR threshold

2.5.3. Voltage regulator

The regulator has three operating modes:

- Main regulator (MR) is used in normal operating mode (Run).
- Low power regulator (LPR) provides an option for even lower power consumption in Stop mode.
- Deep low power regulator (DLP) achieves lower power consumption in Deep stop and Hibernate mode.

2.5.4. Low-power mode

In addition to the normal operating mode, there are other four low-power modes:

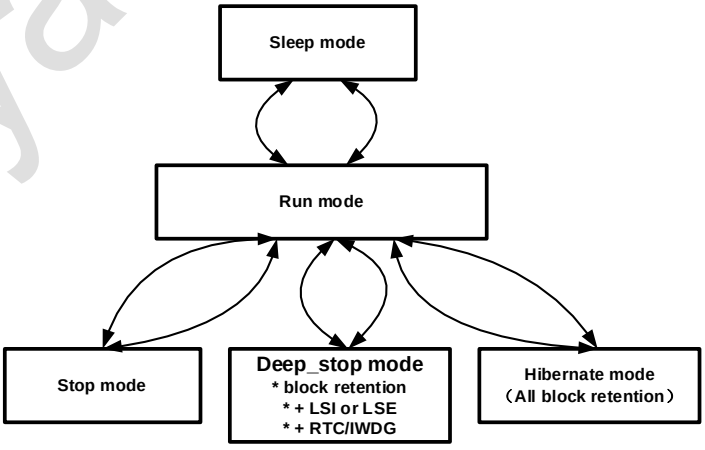

Figure 2-4 Low-power mode

- **Sleep mode：** Peripherals can be configured to keep working when the CPU clock is off (NVIC, SysTick, etc.). It is recommended only to enable the modules that must work, and close the module after the module works.

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- **Stop mode：** LDO enters low-power mode. SRAM and register contents are retained. HSI and HSE are turned off and most module clocks in the V_{DD} domain are disabled.
- **Deep_stop mode：** The LDO enters low-power mode. SRAM and register contents are retained. HSI and HSE are turned off and most module clocks in the V_{DD} domain are disabled. LSI and LSE are software-configurable.
- **Hibernate mode:** The LDO enters HIB mode. SRAM and register contents are retained. HSI and HSE are turned off and most module clocks in the V_{DD} domain are disabled. LSI and LSE can be disabled via software.

2.6. Reset

Two resets are designed in the device: power reset and system reset.

2.6.1. Power reset

A power reset occurs in the following situations:

- Power-on/power-down reset (POR/PDR)
- Brown-out reset (BOR)

2.6.2. System reset

A system reset occurs when the following events occur:

- Reset of NRST pin
- Independent watchdog reset (IWDG)
- SYSRESETREQ software reset
- Option byte load reset (OBL)

2.7. General-purpose inputs and outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (floating, pull-up or pull-down and analog) or as peripheral alternate function. The I/O configuration can be locked and LCD 1/2 Bias output is also supported.

2.8. Interrupts and events

The PY32T020 handles exceptions through the Cortex-M0+ processor's embedded a nested vectored interrupt controller (NVIC) and an extended interrupt/event controller (EXTI).

2.8.1. Nested vectored interrupt controller (NVIC)

NVIC is a tightly coupled IP inside the Cortex-M0+ processor. The NVIC can handle non-maskable interrupts (NMI) and maskable external interrupts from outside the processor and Cortex-M0+ internal exceptions. NVIC provides flexible priority management.

The tight coupling of the processor core to the NVIC greatly reduces the delay between an interrupt event and the initiation of the corresponding interrupt service routine (ISR). The ISR vectors are listed in a vector table, stored at a base address of the NVIC. The vector table base address determines the vector address of the ISR to execute, and the ISR is used as the offset composed of serial numbers.

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If a higher-priority interrupt event occurs and a lower-priority interrupt event is just waiting to be serviced, the later-arriving higher-priority interrupt event will be serviced first. Another optimization is called tail-chaining. When returning from a higher-priority ISR and then starting a pending lower-priority ISR, unnecessary pushes and pops of processor contexts will be skipped. This reduces latency and improves power efficiency.

NVIC features:

- Low latency interrupt handling
- Level 4 interrupt priority
- Support 1 NMI interrupt
- Support up to 26 maskable external interrupts
- Support 10 Cortex-M0+ exceptions
- High-priority interrupts can interrupt low-priority interrupt responses
- Support tail-chaining optimization
- Hardware interrupt vector retrieval

2.8.2. Extended interrupt/event controller (EXTI)

EXTI adds flexibility to handle physical wire events and generates wakeup events/interrupts when waking the processor from Stop/Deep_stop/Hibernate modes.

The EXTI controller has multiple channels, including a maximum of 26 GPIOs, two COMP outputs, RTC, I^2C and TK wake-up signals. GPIO and COMP can be configured to be triggered by a rising edge, falling edge or double edge.

- Each EXTI line can be independently masked through registers.
- The EXTI controller can capture pulses shorter than the internal clock period.
- Registers in the EXTI controller latch each event. Even in Stop/Deep_stop/Hibernate mode, after the processor wakes up from Stop mode, it can identify the wake-up source.

2.9. Analog-to-digital converter (ADC)

The PY32T020 has a 12-bit SARADC. The module has a total of up to 13 channels to be measured, including 10 external and 3 internal channels. The ADC internal voltage reference: V_{REFBUF} (0.6V, 1.5 V, 2.048 V, 2.5 V) or the power supply voltage V_{CC}.

The internal channels are： T_{S_VIN},V_{REFINT} and V_{CC}/3.

A/D conversion of the various channels can be performed in single, continuous, scan or discontinuous mode. The result of the ADC is stored in a left-aligned or right-aligned 16-bit data register.

The analog watchdog feature allows the application to detect if the input voltage goes outside the user-defined higher or lower thresholds.

An efficient low-power mode is implemented to allow very low consumption at low frequency.

Interrupt requests are triggered by the following events: end of sampling, conversion, continuous conversion and analog watchdog threshold violation (converted voltage exceeds preset limits).

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2.10. Touch Key

The PY32T020 integrates a 26 channel capacitive touch circuit:

- Optional internal/external CMOD capacitor, no external capacitor needed for internal use
- High-sensitivity design enables non-contact touch sensing
- 10 V dynamic CS test-passed anti-interference mode
- Support the frequency hopping function
- Support the waterproof compensation function
- Support multi-channel parallel connection
- Support low-power modes: Touch operation in low-power mode maintains total device power consumption < 8 μA

2.11. Comparators (COMP)

General purpose comparators are integrated in the device, which can be used in combination with Timer. Comparators can be used as:

- Triggered by analog signal to wake-up function from low-power mode
- Analog signal conditioning
- Cycle by cycle current control loop when comparators are connected with PWM output from timer.

2.11.1. COMP features

- Each comparator has configurable positive or negative input for flexible voltage selection:
  - Multiple I/O pins
  - Power supply V_{CC} and 64 submultiple values (1/64, 2/64 … 64/64) provided by voltage divider
  - Internal reference voltage is 0.6V, 1.5 V, 2.048 V or 2.5 V， and 64 submultiple values (1/64, 2/64 … 64/64) provided by voltage divider
- The output can be triggered by a connection to the I/O or timer input
  - OCREF_CLR event (cycle by cycle current control)
  - Brakes for fast PWM shutdown
- Each COMP has interrupt generation capability and is used to wake up the device from low power mode (Sleep/Stop) (via EXTI)

2.12. Timers

The different timers feature as blow:

Table 2-3 Timer characteristics

Timer type	Timers	Counter resolution	Counter type	Prescaler	Capture/compare channels	Complementary outputs
Advanced control	TIM1	16-bit	Up, down, up/down	1 - 65536	4	3
General purpose	TIM14	16-bit	Up	1 - 65536	1	-

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2.12.1. Advanced control timer

The advanced-control timer (TIM1) is consist of a 16-bit auto-reload counter driven by a programmable prescaler. It can be used in various scenarios, including pulse length measurement of input signals (input capture) or generating output waveforms (output compare, output PWM, complementary PWM with dead-time insertion).

The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned mode)
- Single pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0 - 100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers by the timer link feature for synchronization or event chaining.

2.12.2. General purpose timer

The general-purpose timer TIM14 is consist of a 16-bit auto-reload counter driven by a programmable prescaler.

TIM14 features one single channel for input capture/output compare, PWM or one-pulse mode output.

The counter can be frozen in debug mode.

2.12.3. Independent watchdog (IWDG)

Independent watchdog (IWDG) is integrated in the device, and this module has the characteristics of high-security level, accurate timing and flexible use. IWDG finds and resolves functional confusion due to software failure and triggers a system reset when the counter reaches the specified timeout value.

The IWDG is clocked by LSI, so even if the main clock fails, it can keep working.

IWDG is the best suited for applications that require the watchdog as a standalone process outside of the main application and do not have high timing accuracy constraints.

Controlling of option byte can enable IWDG hardware mode.

IWDG is the wake-up source of Stop mode, which wakes up Stop mode by reset.

The counter can be frozen in debug mode.

2.12.4. SysTick timer

SysTick timer is dedicated to real-time operating systems (RTOS), but could also be used as a standard down counter.

SysTick features:

- A 24-bit down counter

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- Auto-reload capability
- Maskable system interrupt generation when the counter reaches 0

2.13. Real-time clock (RTC)

The RTC is an independent counter. It has a set of continuous counting counters, which can provide a clock calendar function under the corresponding software configuration. Modifying the value of the counter can reset the current time and date of the system.

- RTC is a 32-bit programmable counter with a prescaler factor of up to 220 bits.
- RTC counter clock source can be LSE/LSI and HSE/128, also can be the stop wake-up source.
- RTC can generate alarm interrupt, second interrupt and overflow interrupt (maskable).
- RTC supports clock calibration.
- RTC can be frozen in debug mode.

2.14. Inter-integrated circuit interface (I^2C)

The I^2C (inter-integrated circuit) bus interface handles communications between the microcontroller and the serial I^2C bus. It provides multimaster capability, and controls all I^2C bus-specific sequencing, protocol, arbitration and timing. Standard mode (Sm), Fast mode (Fm) and Fast mode plus (Fm+) are supported.

I^2C features:

- Multimaster capability : can be master or slave
- Support different communication speeds
  - Standard mode (Sm): up to 100 kHz
  - Fast mode (Fm): up to 400 kHz
  - Fast mode plus (Fm+): up to 1 MHz
- As master
  - Generate Clock
  - Generation of Start and Stop
- As slave
  - Programmable I^2C address detection
  - Discovery of the Stop bit
- 7-bit addressing mode
- General call
- Status flag
  - Transmit/receive mode flags
  - Byte transfer complete flag
  - I^2C busy flag bit
- Error flag
  - Master arbitration loss
  - ACK failure after address/data transfer

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  - Start/Stop error
  - Overrun/Underrun (clock stretching function disable)
- Optional clock stretching
- Software reset
- Analog noise filter function
- Low-power address matching wake-up

2.15. Universal Asynchronous Receivers/Transmitter (UART)

The UARTs provide a flexible method for full-duplex data exchange with external devices using the industry-standard NRZ asynchronous serial data format. The UART utilizes a fractional baud rate generator to provide a wide range of baud rate options.

Automatic baud rate detection is supported.

UART features:

- Support 5/6/7/8/9 bits serial data
- Support 1/2 STOP bits (1/1.5 STOP bits for 5 bits data)
- Support sending address/data
- Support fixed parity check
- Support break frames
- Detect start bit errors
- Support programmable fractional baud rate: The serial data baud rate is programmable and derived from the formula: Baud Rate = Serial Clock Frequency / (16 × Divisor).
- Support SWAP function
- Support MSBFIRST endianness switching

2.16. Serial peripheral interface (SPI)

SPIs allow the device to communicate with external devices in half-duplex, full-duplex, and simplex synchronous serial communication. This interface can be configured in Master mode and provides the serial clock (SCK) for external slave devices. The interface can also work in a multi-master configuration.

The SPI features are as follows:

- Master or slave mode
- Full-duplex synchronous transfers on three lines
- Half-duplex synchronous transfer on two lines (with bidirectional data line)
- Simplex synchronous transfers on two lines (with unidirectional data line)
- 8-bit or 16-bit transmission frame selection
- Support multi-master mode
- 8 master mode baud rate prescale factors (Max 24 M)
- Slave mode frequency (Max 24 M)
- Both master and slave modes can be managed by software or hardware NSS: dynamic change of master/slave operating mode

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- Programmable clock polarity and phase
- Programmable data order with MSB-first or LSB-first shifting
- Dedicated transmission and reception flags with interrupt capability
- SPI bus busy status flag
- Support Motorola mode
- Master mode fault, overrun flags with interrupt capability
- Two 32-bit Rx and Tx FIFOs

2.17. Serial wire debug (SWD)

An ARM SWD interface allows serial debugging tools to be connected to the PY32T020.

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3. Pinouts and pin descriptions

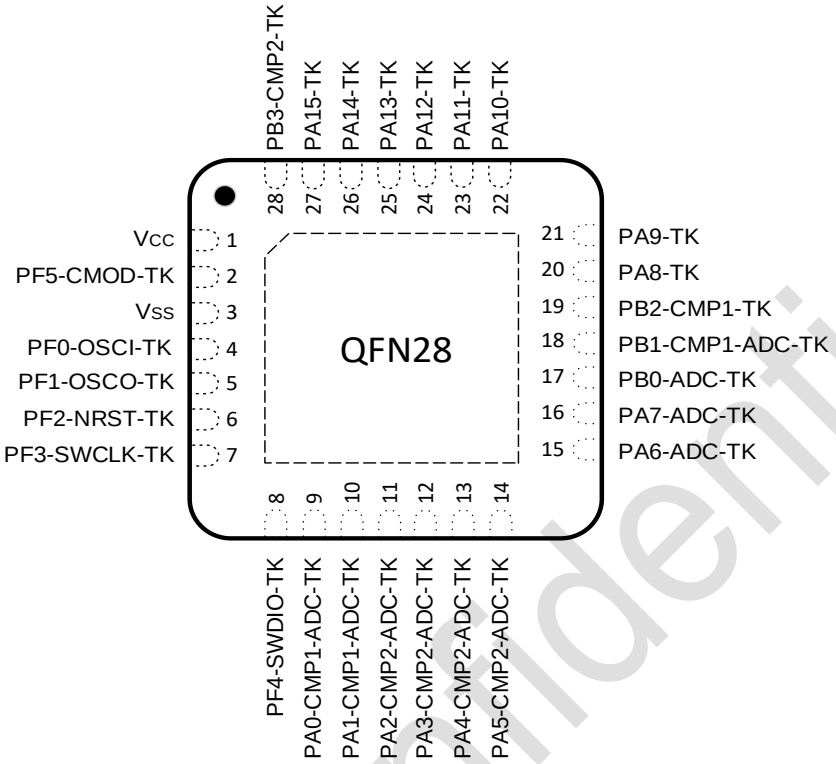

Figure 3-1 QFN28 Pinout1 PY32T020G1xU7 (Top view)

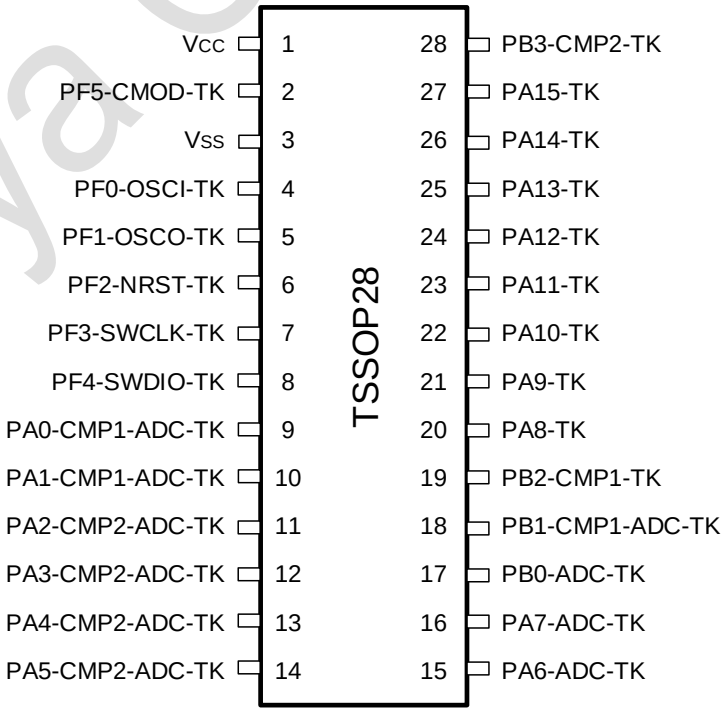

Figure 3-2 TSSOP28 Pinout1 PY32T020G1xP7 (Top view)

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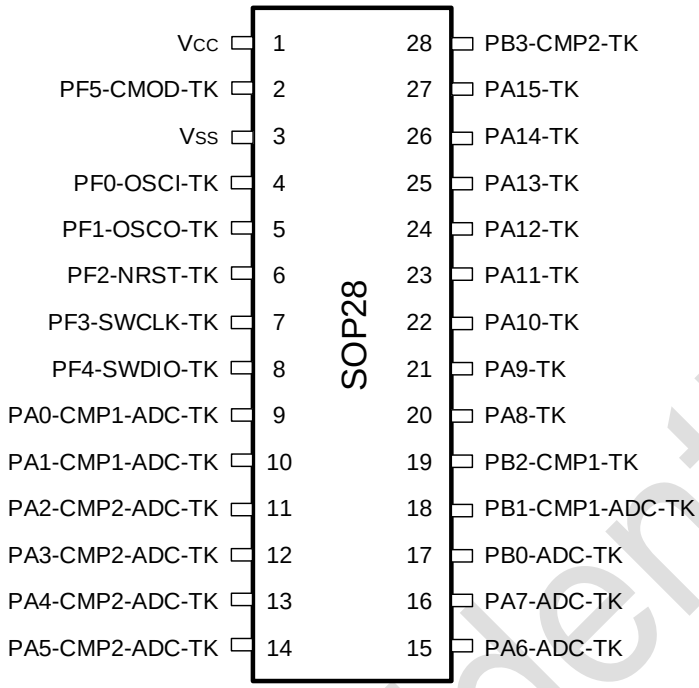

Figure 3-3 SOP28 Pinout1 PY32T020G1xS7 (Top view)

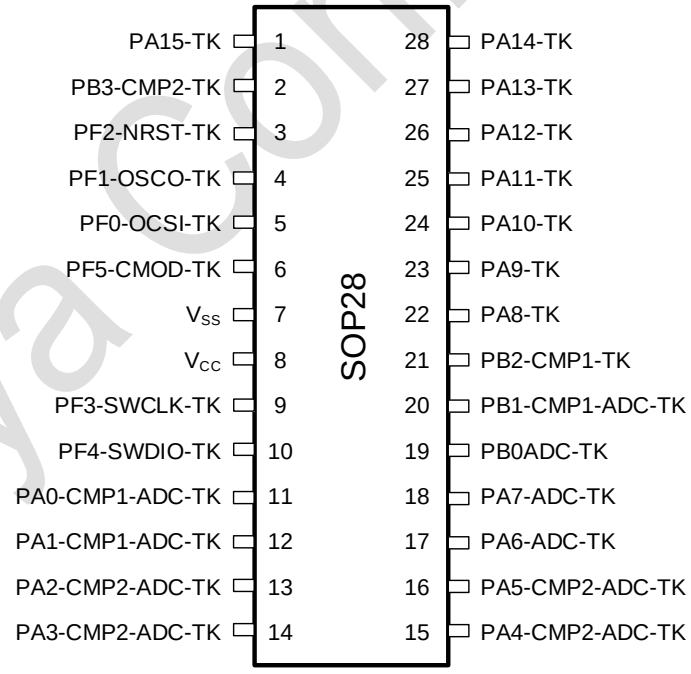

Figure 3-4 SOP28 Pinout2 PY32T020G2xS7 (Top view)

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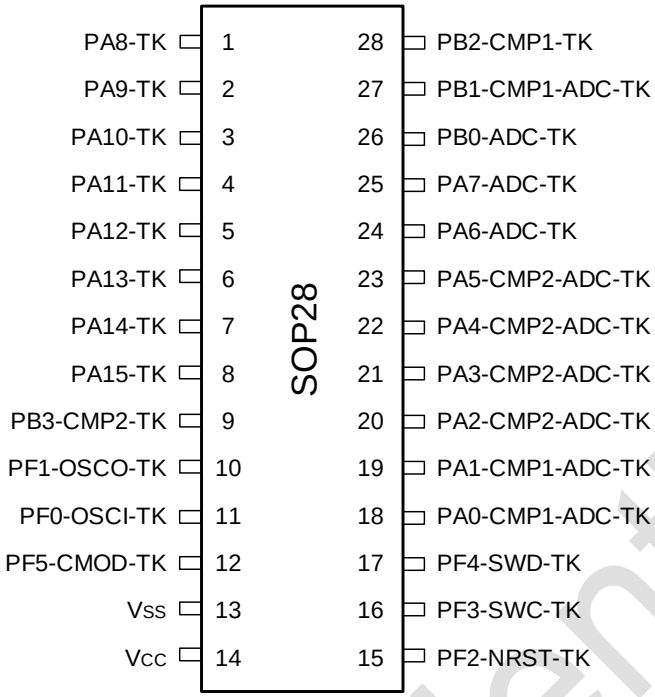

Figure 3-5 SOP28 Pinout3 PY32T020G3xS7 (Top view)

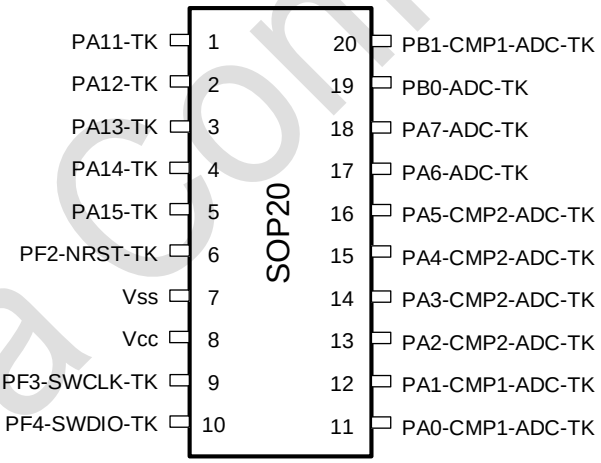

Figure 3-6 SOP20 Pinout2 PY32T020F2xS7 (Top view)

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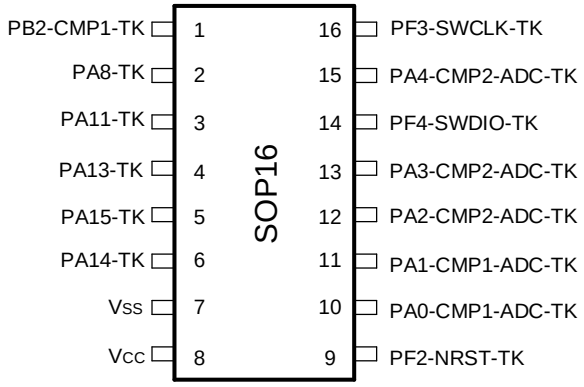

Figure 3-7 SOP16 Pinout1 PY32T020W1xS7 (Top view)

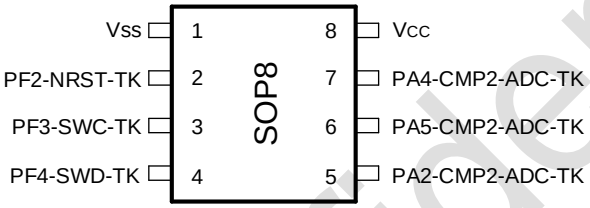

Figure 3-8 SOP8 Pinout1 PY32T020L1xS7 (Top view)

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Table 3-1 Legend/abbreviations used in the pinout table

Timer type		Symbol	Definition
Pin type		S	Supply pin
		G	Ground pin
		I/O	Input / output pin
		NC	No internal connection
I/O structure		COM	Standard 5 V I/O, with analog switch function
		RST	Bidirectional reset pin with embedded weak pull-up resistor
		_L	LED COM port supports 80 mA sink current and analog input/output functions
		_C	LED SEG port supports constant - current drive and analog input/output functions
		_F	I/O, I^2C SCL SDA capable with analog input and output function
		_P	Support 2.7 V 20 mA, 5 V 30 mA source current, analog input and output functions
Notes		-	Unless otherwise specified, all ports are used as analog inputs be- tween and after reset All I/Os support Touch Key Cap sense ports and analog input/output functions. All I/Os support LCD 1/2 Bias output function.
Pin functions	Alternate functions	-	Function selected through GPIOx_AFR register
	Additional functions	-	Functions directly selected/enabled through peripheral registers

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Table 3-2 Pin definitions[5]

Packages								Reset	Pin type	I/O structure	Port function[8]	
QFN28 G1	TSSOP28 G1	SOP28 G1	SOP28 G2	SOP28 G3	SOP20 F2	SOP16 W1	SOP8 L1				Multiplexed function[6]	Additional functions
1	1	1	8	14	8	8	8	V_{CC}	S	-	Power Supply	
2	2	2	6	12	-	-	-	PF5-CMOD	I/O	COM	-	TK_CMOD TK_IN25
3	3	3	7	13	7	7	1	V_{SS}	G	-	Ground	
4	4	4	5	11	-	-	-	PF0-OSCI[9]	I/O	COM	TM14_CH1	OSCIN TK_IN24
5	5	5	4	10	-	-	-	PF1-OSCO[9]	I/O	COM	TM14_CH1	OSCOUT TK_IN23
6	6	6	3	15	6	9	2	PF2-NRST[4]	I/O	RST COM_F	I2C_SCL TM14_CH1 MCO	NRST TK_IN22
7	7	7	9	16	9	16	3	PF3-SWCLK[1][2][3][7]	I/O	COM_F	UART1_TX I2C_SDA I2C_SCL TM1_ETR TM14_CH1 SWCLK	TK_IN21
8	8	8	10	17	10	14	4	PF4-SWDIO[1][2][3][7]	I/O	COM_F	UART1_RX I2C_SCL	TK_IN20

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Packages								Reset	Pin type	I/O structure	Port function(8)	
QFN28 G1	TSSOP28 G1	SOP28 G1	SOP28 G2	SOP28 G3	SOP20 F2	SOP16 W1	SOP8 L1				Multiplexed function(6)	Additional functions
											I2C_SDA	
											TM1_ETR	
											TM14_CH1	
											SWDIO	
9	9	9	11	18	11	10	-	PA0	I/O	COM_C	SPI_NSS	CMP1_INM ADC_IN0 TK_IN19
											UART2_TX	
											TM1_CH1N	
											TM1_CH3	
											CMP1_OUT	
10	10	10	12	19	12	11	-	PA1	I/O	COM_C	SPI_SCK	CMP1_INP ADC_IN1 TK_IN18
											UART2_RX	
											TM1_CH2N	
											TM1_CH4	
											EVENTOUT	
											MCO	
11	11	11	13	20	13	12	5	PA2	I/O	COM_P	SPI_MOSI	CMP2_INM ADC_IN2 TK_IN17
											UART3_TX	
											TM14_CH1	
12	12	12	14	21	14	13	-	PA3	I/O	COM	SPI_MISO	CMP2_INP ADC_IN3
											UART3_RX	

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Packages								Reset	Pin type	I/O structure	Port function(8)	
QFN28 G1	TSSOP28 G1	SOP28 G1	SOP28 G2	SOP28 G3	SOP20 F2	SOP16 W1	SOP8 L1				Multiplexed function(6)	Additional functions
											TM1_CH1	TK_IN16
											EVENTOUT	
13	13	13	15	22	15	15	7	PA4	I/O	COM	SPI_NSS	CMP2_INP ADC_IN4 TK_IN15
											UART2_TX	
											TM1_CH3	
											RTC_OUT	
14	14	14	16	23	16	-	6	PA5	I/O	COM_C	SPI_SCK	CMP2_INP ADC_IN5 TK_IN14
											UART2_RX	
											TM1_CH2	
											MCO	
15	15	15	17	24	17	-	-	PA6	I/O	COM_C	SPI_MISO	ADC_IN6 TK_IN13
											UART1_TX	
											TM1_BKIN	
											TM1_CH1	
											CMP1_OUT	
16	16	16	18	25	18	-	-	PA7	I/O	COM_C COM_P	SPI_MOSI	ADC_IN7 TK_IN12
											UART1_RX	
											TIM1_CH1N	
											RTC_OUT	
											CMP2_OUT	

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Packages								Reset	Pin type	I/O structure	Port function(8)	
QFN28 G1	TSSOP28 G1	SOP28 G1	SOP28 G2	SOP28 G3	SOP20 F2	SOP16 W1	SOP8 L1				Multiplexed function(6)	Additional functions
											EVENTOUT	
17	17	17	19	26	19	-	-	PB0	I/O	COM	SPI_NSS	ADC_IN8 TK_IN11
											UART2_TX	
											TIM1_CH2N	
											CMP1_OUT	
18	18	18	20	27	20	-	-	PB1	I/O	COM	UART2_RX	CMP1_INM ADC_IN9 TK_IN10
											TIM1_CH3N	
											EVENTOUT	
19	19	19	21	28	-	1	-	PB2	I/O	COM_C	SPI_MISO	CMP1_INP TK_IN9
											UART3_RX	
											TM14_CH1	
20	20	20	22	1	-	2	-	PA8	I/O	COM_C COM_F	SPI_MOSI	TK_IN8
											UART3_TX	
											I2C_SDA	
											TIM1_CH1	
											MCO	
21	21	21	23	2	-	-	-	PA9	I/O	COM	UART2_TX	TK_IN7
											TM1_ETR	
											TM1_BKIN	
											TM14_CH1	

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Packages								Reset	Pin type	I/O structure	Port function(8)	
QFN28 G1	TSSOP28 G1	SOP28 G1	SOP28 G2	SOP28 G3	SOP20 F2	SOP16 W1	SOP8 L1				Multiplexed function(6)	Additional functions
											EVENTOUT	
22	22	22	24	3	-	-	-	PA10	I/O	COM	UART2_RX	TK_IN6
											TM1_CH3	
											TM14_CH1	
23	23	23	25	4	1	3	-	PA11	I/O	COM_F COM_L	SPI_SCK	TK_IN5
											UART1_TX	
											I2C_SCL	
											TIM1_CH4	
24	24	24	26	5	2	-	-	PA12	I/O	COM_L	SPI_MOSI	TK_IN4
											UART1_RX	
											TM1_ETR	
											TM14_CH1	
											EVENTOUT	
25	25	25	27	6	3	4	-	PA13(SWDIO)(1)(2)(3)	I/O	COM_L	SWDIO	TK_IN3
											UART2_TX	
											TM1_CH3N	
											MCO	
26	26	26	28	7	4	6	-	PA14(SWCLK)(1)(2)(3)	I/O	COM_L	SWCLK	TK_IN2
											UART3_TX	
											TM1_CH2N	

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Packages								Reset	Pin type	I/O structure	Port function(8)	
QFN28 G1	TSSOP28 G1	SOP28 G1	SOP28 G2	SOP28 G3	SOP20 F2	SOP16 W1	SOP8 L1				Multiplexed function(6)	Additional functions
											EVENTOUT	
27	27	27	1	8	5	5	-	PA15	I/O	COM_L	SPI_NSS	TK_IN1
											UART3_RX	
											TM1_CH1N	
											TM1_CH4	
28	28	28	2	9	-	-	-	PB3	I/O	COM_C	SPI_SCK	CMP2_INM TK_IN0
											UART2_RX	
											TM1_CH2	

1. PA3, PA4, PA13, and PA14 can be configured via options to select GPIO functionality or SWC/SWD functionality.

option[1:0]	PF3	PF4	PA13	PA14
0/0(default)	SWCLK	SWDIO	GPIO	GPIO
0/1	GPIO	GPIO	SWDIO	SWCLK
1/0	GPIO	SWDIO	GPIO	SWCLK
1/1	SWCLK	GPIO	SWDIO	GPIO

2. After reset, when the option byte is configured to 0/0 (default state), PF3 and PF4 are configured as SWCLK and SWDIO.
3. The internal pull-up resistor is activated when configured as SWDIO and the internal pull-down resistor is activated when configured as SWCLK.
4. Configured by option bytes to choose GPIO or NRST.
5. All IOs support pull-up, pull-down valid at the same time, output 1/2 V_{CC} level.
6. The RX/TX of UART1, UART2, and UART3 can be set to be interchangeable within the IP.

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7. When used as a closed I^2C EEPROM, an internal pull-up resistor of 4.7 kΩ can be configured.
8. TK function and GPIO digital function cannot be turned on at the same time.
9. When HSE_ON is enabled, the crystal oscillator is used for HSE. When LSE_ON is enabled, the crystal oscillator is used for LSE. HSE_ON and LSE_ON cannot be enabled simultaneously.

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3.1. Alternate functions selected through GPIOA_AFR registers for port A

Table 3-3 Port A alternate functions mapping

PortA	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	SPI_NSS	-	TM1_CH3	UART2_TX	-	TM1_CH1N	CMP1_OUT	-
PA1	SPI_SCK	-	TM1_CH4	UART2_RX	-	TM1_CH2N	MCO	EVENTOUT
PA2	SPI_MOSI	UART3_TX		-	-	TM14_CH1	-	-
PA3	SPI_MISO	UART3_RX	TM1_CH1	-	-	-	-	EVENTOUT
PA4	SPI_NSS	-	TM1_CH3	UART2_TX	RTC_OUT	-	-	-
PA5	SPI_SCK	-	TM1_CH2	UART2_RX	-		MCO	-
PA6	SPI_MISO	UART1_TX	TM1_CH1	-	-	TM1_BKIN	CMP1_OUT	-
PA7	SPI_MOSI	UART1_RX	TM1_CH1N	-	RTC_OUT	TM1_CH1	CMP2_OUT	EVENTOUT
PA8	SPI_MOSI	UART3_TX	TM1_CH1	-	I2C_SDA	-	MCO	-
PA9	-	-	TM1_ETR	UART2_TX	-	TM1_BKIN	TM14_CH1	EVENTOUT
PA10	-	-	TM1_CH3	UART2_RX	-	TM14_CH1	-	-
PA11	SPI_SCK	UART1_TX	TM1_CH4	-	I2C_SCL	-	-	-
PA12	SPI_MOSI	UART1_RX	TM1_ETR	-	-	TM14_CH1	-	EVENTOUT
PA13	SWDIO	-	TM1_CH3N	UART2_TX	-	-	MCO	-
PA14	SWCLK	UART3_TX	TM1_CH2N	-	-	-	-	EVENTOUT
PA15	SPI_NSS	UART3_RX	TM1_CH1N	-	-	TM1_CH4	-	-

3.2. Alternate functions selected through GPIOB_AFR registers for port B

Table 3-4 Port B alternate function mapping

PortB	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB0	SPI_NSS	-	TM1_CH2N	UART2_TX	-	TM1_CH2	CMP1_OUT	-
PB1	-	-	TM1_CH3N	UART2_RX	-	-	-	EVENTOUT
PB2	SPI_MISO	UART3_RX	-	-	-	TM14_CH1	-	-
PB3	SPI_SCK	-	TM1_CH2	UART2_RX	-	-	-	-

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3.3. Alternate functions selected through GPIOF_AFR registers for port F

Table 3-5 Port F alternate function mapping

PortF	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PF0	-	-	-	-	-	TM14_CH1	-	-
PF1	-	-	-	-	-	TM14_CH1	-	-
PF2	-	-	-	-	I2C_SCL	TM14_CH1	MCO	-
PF3	SWCLK	UART1_TX	TM1_ETR	I2C_SCL	I2C_SDA	TM14_CH1	-	-
PF4	SWDIO	UART1_RX	TM1_ETR	I2C_SCL	I2C_SDA	TM14_CH1	-	-
PF5	-	-	-	-	-	-	-	-

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4. Memory mapping

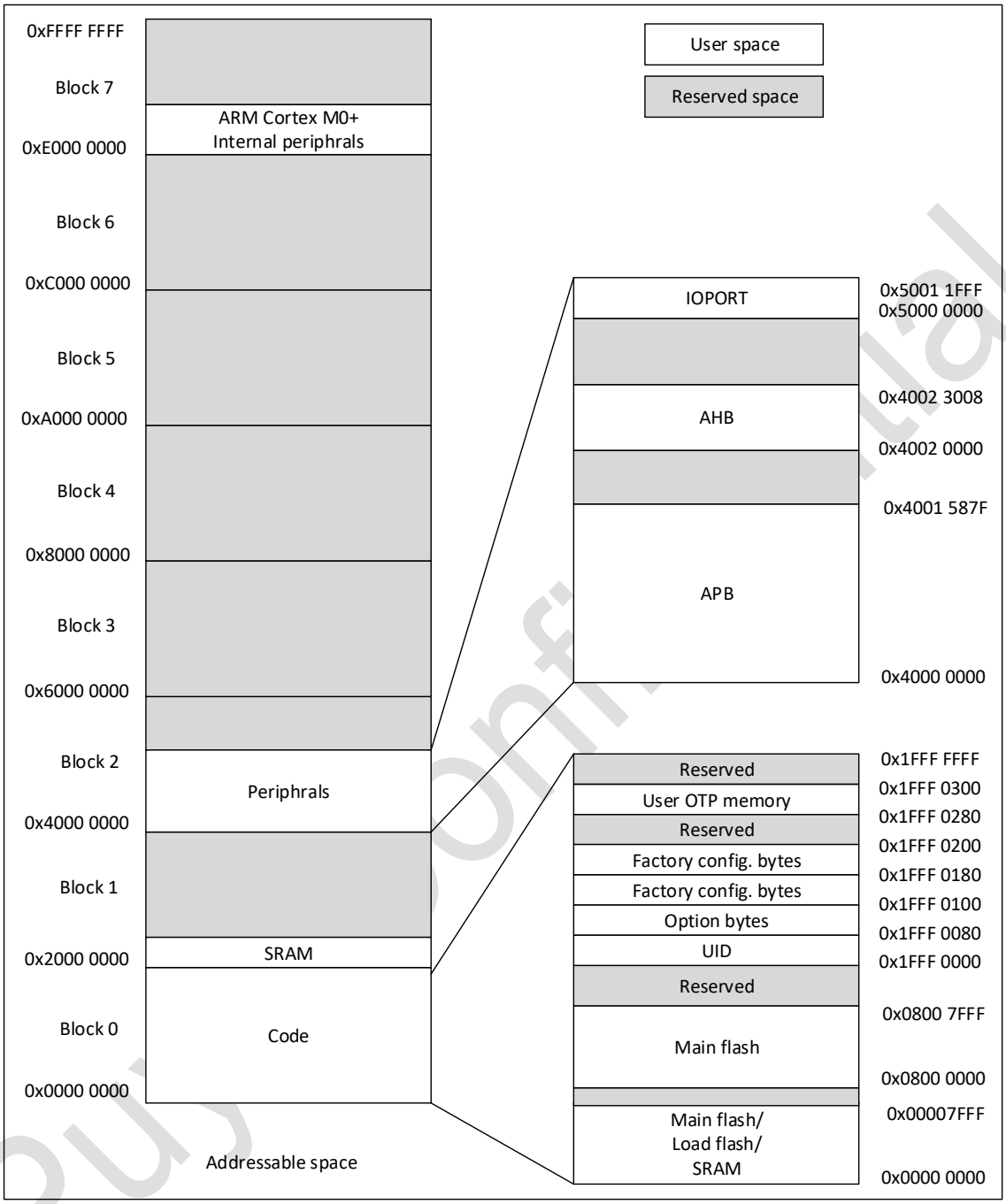

Figure 4-1 Memory map

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Table 4-1 Memory boundary address

Type	Boundary Address	Size	Memory Area (1)
SRAM	0x2000 1000-0x3FFF FFFF	-	Reserved(1)
	0x2000 0000-0x2000 0FFF	4 KB	SRAM
Code	0x1FFF 0300-0x1FFF FFFF	-	Reserved
	0x1FFF 0280-0x1FFF 02FF	128 Bytes	USER OTP memory
	0x1FFF 0180-0x1FFF 01FF	128 Bytes	Factory config. bytes
	0x1FFF 0100-0x1FFF 017F	128 Bytes	Factory config. bytes
	0x1FFF 0080-0x1FFF 00FF	128 Bytes	Option bytes
	0x1FFF 0000-0x1FFF 007F	128 Bytes	UID
	0x0800 8000-0x1FFE FFFF	-	Reserved
	0x0800 0000-0x0800 7FFF	32 KB	Main flash memory
	0x0000 8000-0x07FF FFFF	-	Reserved
	0x0000 0000-0x0000 7FFF	32 KB	Selection based on Boot configuration: 1. Main flash memory 2. Load flash 3. SRAM

1. The address is marked as Reserved, which cannot be written, read as 0, and a response error is generated.

Table 4-2 Peripheral register address

Bus	Boundary Address	Size	Peripheral (1)
	0xE000 0000-0xE00F FFFF	1 MB	M0+
IOPORT	0x5000 1800-0x5FFF FFFF	-	Reserved(1)
	0x5000 1400-0x5000 17FF	1 KB	GPIOF
	0x5000 0800-0x5000 13FF	-	Reserved(1)
	0x5000 0400-0x5000 07FF	1 KB	GPIOB
	0x5000 0000-0x5000 03FF	1 KB	GPIOA
AHB	0x4002 3400-0x4FFF FFFF	-	Reserved
	0x4002 3010-0x4002 33FF	1 KB	Reserved
	0x4002 3000-0x4002 300F		CRC
	0x4002 2400-0x4002 2FFF	-	Reserved
	0x4002 2000-0x4002 23FF	1 KB	Flash FMC
	0x4002 1C00-0x4002 1FFF	-	Reserved
	0x4002 1900-0x4002 1BFF	1 KB	Reserved
	0x4002 1800-0x4002 18FF		EXTI(2)
	0x4002 1400-0x4002 17FF	-	Reserved
	0x4002 1080-0x4002 13FF	1 KB	Reserved
	0x4002 1000-0x4002 107F		RCC(2)

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Bus	Boundary Address	Size	Peripheral (1)
	0x4002 0000-0x4002 0FFF	-	Reserved
APB	0x4001 5C00-0x4001 FFFF	-	Reserved
	0x4001 5880-0x4001 5BFF	1 KB	Reserved
	0x4001 5800-0x4001 587F		DBG
	0x4001 4800-0x4001 57FF	-	Reserved
	0x4001 4480-0x4001 47FF	1 KB	Reserved
	0x4001 4400-0x4001 447F		UART2
	0x4001 3C00-0x4001 43FF	-	Reserved
	0x4001 3880-0x4001 3BFF	1 KB	Reserved
	0x4001 3800-0x4001 387F		UART3
	0x4001 3400-0x4001 37FF	-	Reserved
	0x4001 3080-0x4001 33FF	1 KB	Reserved
	0x4001 3000-0x4001 307F		SPI
	0x4001 2C80-0x4001 2FFF	1 KB	Reserved
	0x4001 2C00-0x4001 2C7F		TIM1
	0x4001 2800-0x4001 2BFF	-	Reserved
	0x4001 2400-0x4001 27FF	1 KB	ADC
	0x4001 0400-0x4001 23FF	-	Reserved
	0x4001 0220-0x4001 03FF	1 KB	Reserved
	0x4001 0200-0x4001 021F		CMP1/2
	0x4001 0000-0x4001 01FF		SYSCFG
	0x4000 7400-0x4000 FFFF	-	Reserved
	0x4000 7080-0x4000 73FF	1 KB	Reserved
	0x4000 7000-0x4000 707F		PWR(3)
	0x4000 5800-0x4000 6FFF	-	Reserved
	0x4000 5480-0x4000 57FF	1 KB	Reserved
	0x4000 5400-0x4000 547F		I^2C
	0x4000 4800-0x4000 53FF	-	Reserved
	0x4000 4480-0x4000 47FF	1 KB	Reserved
	0x4000 4400-0x4000 447F		UART1
	0x4000 3C00-0x4000 43FF	-	Reserved
	0x4000 3880-0x4000 3BFF	1 KB	Reserved
	0x4000 3800-0x4000 387F		TK
	0x4000 3400-0x4000 37FF	-	Reserved
	0x4000 3080-0x4000 33FF	1 KB	Reserved
	0x4000 3000-0x4000 307F		IWDG
	0x4000 2C00-0x4000 2FFF	-	Reserved
	0x4000 2880-0x4000 2BFF	1 KB	Reserved

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Bus	Boundary Address	Size	Peripheral (1)
	0x4000 2800-0x4000 287F		RTC
	0x4000 2400-0x4000 27FF	-	Reserved
	0x4000 2080-0x4000 23FF	1 KB	Reserved
	0x4000 2000-0x4000 207F		TIM14
	0x4000 0000-0x4000 1FFF	-	Reserved

1. In the above table, the reserved address cannot be written, read back is 0, and a hard fault is generated
2. Not only supports 32-bit word access, but also supports half-word and byte access.
3. Not only supports 32-bit word access, but also supports half-word access.

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5. Electrical characteristics

5.1. Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1. Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A =25 °C and T_A =$T_{A(max)}$ (given by the selected temperature range).

Data based on electrical characterization results, design simulations and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation.

5.1.2. Typical values

Unless otherwise specified, typical data is based on T_A =25 °C and V_{CC} = 3.3 V. These data are for design guidance only and have not been tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated.

5.1.3. Power supply scheme

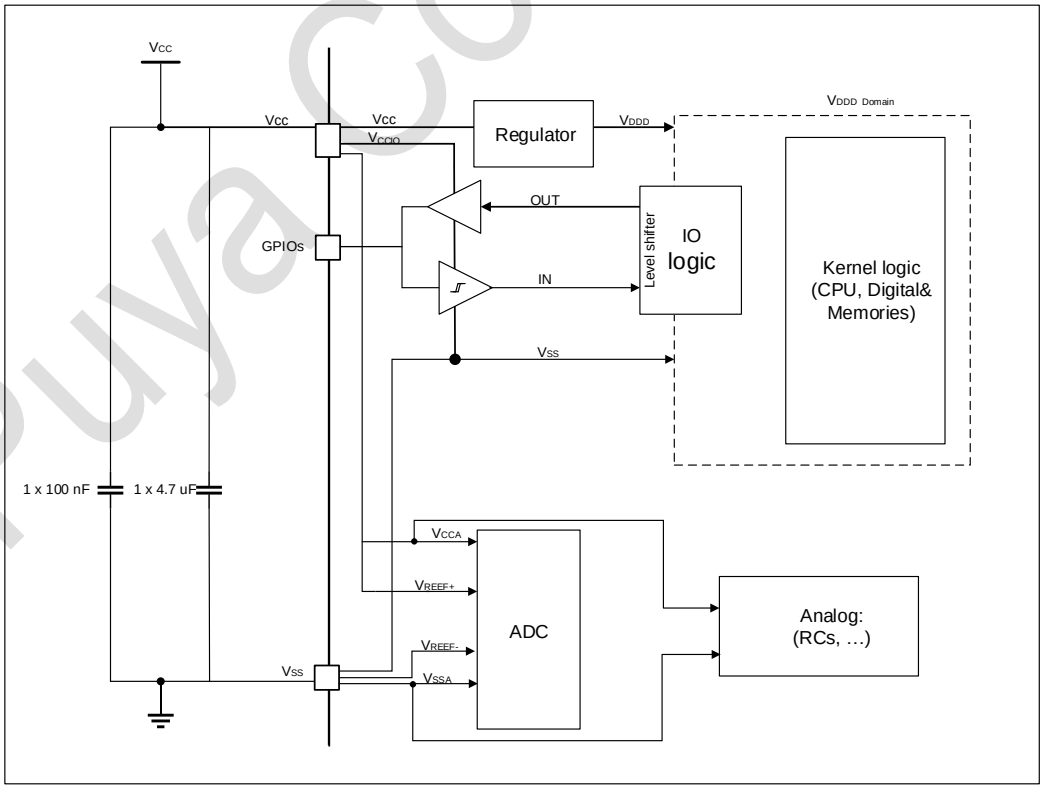

Figure 5-1 Power supply scheme

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5.2. Absolute maximum ratings

Stresses above the absolute maximum ratings listed in following tables may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5-1 Voltage characteristics(1)

Symbol	Ratings	Min	Max	Unit
V_{CC}-V_{SS}	External main power supply(1)	-0.3	6.25	V
V_{IN}(2)	Input voltage on any other pin	V_{SS} - 0.3	V_{CC} + 0.3	

1. Main power V_{CC} and ground V_{SS} pins must always be connected to the external power supply, in the permitted range.
2. Maximum V_{IN} must always follow allowable maximum injection current limits as per the table.

Table 5-2 Current characteristics

Symbol	Ratings	Max	Unit
ΣI_{VCC}	Total current into sum of all V_{CC} power lines (source)(1)	170	mA
ΣI_{VSS}	Total current out of sum of all V_{SS} ground lines (sink)(1)	170	mA
$I_{IO(PIN)}$(2)	Output current sunk by any COM I/O and control pin	30	mA
	Output current sunk by any COM_L I/O and control pin	100	
	Output current source by any COM I/O and control pin	25	
	Output current source by any COM_P I/O and control pin	30	
$\Sigma I_{IO(PIN)}$(2)	Output current sunk by sum of all COM I/Os and control pins	160	mA
	Output current source by sum of all COM I/Os and control pins	150	

1. Main power V_{CC} and ground V_{SS} pins must always be connected to the external power supply, in the permitted range.
2. These I/O types refer to the terms and symbols defined by pins.

Table 5-3 Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 - +150	°C
T_O	Operating temperature range	-40 - +105	°C

5.3. Operating conditions

5.3.1. General operating conditions

Table 5-4 General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	48	MHz
f_{PCLK}	Internal APB clock frequency	-	0	48	MHz
V_{CC}	Standard operating voltage	-	1.8	5.5	V
V_{IN}	I/O input voltage	-	-0.3	V_{CC}+0.3	V
T_A	Ambient temperature	-	-40	105	°C
T_J	Junction temperature	-	-40	110	°C

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5.3.2. Operating conditions at power-on / power-down

Table 5-5 Operating conditions at power-on / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VCC}	V_{CC} rise time rate	-	0	∞	μs/V
	V_{CC} fall time rate	-	20	∞	

5.3.3. Embedded reset

Table 5-6 Embedded reset characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(1)	Reset temporization	-	-	4.00	7.50	ms
$V_{POR/PDR}$	Power-on/power-off reset threshold	Rising edge	1.60(2)	1.70	1.80	V
		Falling edge	1.57	1.67	1.77(2)	
V_{BOR2}	BOR2 threshold	Rising edge	1.89(2)	1.99	2.09	V
		Falling edge	1.78	1.88	1.98(2)	
V_{BOR3}	BOR3 threshold	Rising edge	2.09(2)	2.19	2.29	V
		Falling edge	2.00	2.10	2.20(2)	
V_{BOR4}	BOR4 threshold	Rising edge	2.29(2)	2.39	2.49	V
		Falling edge	2.20	2.30	2.40(2)	
V_{BOR5}	BOR5 threshold	Rising edge	2.66(2)	2.78	2.89	V
		Falling edge	2.58	2.69	2.79(2)	
V_{BOR6}	BOR6 threshold	Rising edge	2.94(2)	3.08	3.18	V
		Falling edge	2.88	2.99	3.11(2)	
V_{BOR7}	BOR7 threshold	Rising edge	3.53(2)	3.68	3.83	V
		Falling edge	3.44	3.58	3.72(2)	
V_{BOR8}	BOR8 threshold	Rising edge	4.03(2)	4.20	4.36	V
		Falling edge	3.91	4.08	4.24(2)	
$V_{POR\_PDR\_hyst}$(1)	POR/PDR hysteresis	-	-	30	-	mV
V_{BOR_hyst}(1)	BOR hysteresis	-		100		mV
$I_{CC(BOR)}$	BOR consumption	-	-	0.6	-	μA

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

5.3.4. Supply current characteristics

Table 5-7 Current consumption in Run mode

Symbol	Conditions						Typ(1)	Max	Unit
	System clock	Frequency	Code	Run	Peripheral Clock	Flash sleep			
I_{CC}(Run)	HSI	48 MHz	While(1)	Flash	ON	DISABLE	2.60	-	mA

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Symbol	Conditions						Typ(1)	Max	Unit
	System clock	Frequency	Code	Run	Peripheral Clock	Flash sleep			
					OFF	DISABLE	1.90	-	
		24 MHz			ON	DISABLE	1.70	-	
					OFF	DISABLE	1.40	-	
	LSI	32.768 kHz			ON	DISABLE	165	-	μA
					OFF	DISABLE	164	-	
		32.768 kHz			ON	ENABLE	92.0	-	
					OFF	ENABLE	91.5	-	

1. Data based on characterization results, not tested in production.

Table 5-8 Current consumption in Sleep mode

Symbol	Conditions				Typ(1)	Max	Unit
	System clock	Frequency	Peripheral Clock	Flash sleep			
I_{CC}(Sleep)	HSI	48 MHz	ON	DISABLE	1.70	-	mA
			OFF	DISABLE	0.90	-	
		24 MHz	ON	DISABLE	1.00	-	
			OFF	DISABLE	0.60	-	
	LSI	32.768 kHz	ON	DISABLE	161	-	μA
			OFF	DISABLE	160	-	
		32.768 kHz	ON	ENABLE	81.3	-	
			OFF	ENABLE	81.0	-	

1. Data based on characterization results, not tested in production.

Table 5-9 Current consumption in Stop mode

Symbol	Conditions				Typ(1)	Max	Unit
	V_{CC}	LDO mode	LSI	Peripheral Clock			
I_{CC}(Stop)	1.8 - 5.5 V	MR	-	-	75.2	-	μA
		LPR	ON	IWDG+RTC	3.90	-	
				IWDG	3.90	-	
				RTC	3.90	-	
			OFF	No	3.50	-	

1. Data based on characterization results, not tested in production.

Table 5-10 Current consumption in Deep_stop mode

Symbol	Conditions				Typ(1)	Max	Unit
	V_{CC}	LDO mode	LSI	Peripheral Clock			
I_{CC}(Deep_stop)	1.8 - 5.5 V	DLP	ON	IWDG+RTC	3.10	-	μA
				IWDG	3.10	-	

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Symbol	Conditions				Typ(1)	Max	Unit
	V_{CC}	LDO mode	LSI	Peripheral Clock			
				RTC	3.10	-	
			OFF	No	3.00	-	

1. Data based on characterization results, not tested in production.

Table 5-11 Current consumption in Hibernate mode

Symbol	Conditions				Typ(1)	Max	Unit
	V_{CC}	LDO mode	LSI	Peripheral Clock			
I_{CC}(Hibernate)	1.8 - 5.5 V	DLP	OFF	No	2.30	-	μA

1. Data based on characterization results, not tested in production.

5.3.5. Wakeup time from low-power mode

Table 5-12 Wakeup time from low-power mode

Symbol	Parameter(1)		Conditions	Typ(2)	Max	Unit
$t_{WUSLEEP}$	Wake-up from Sleep mode		-	10	-	CPU Cycles
t_{WUSTOP}	Wake-up from Stop mode	MR	Run program in Flash, HSI (24 MHz) as system clock FLS_SLPTIME [1:0] = 00	6.6	-	μs
			Run program in Flash, HSI (48 MHz) as system clock FLS_SLPTIME [1:0] = 00	6.1		
		LPR	Run program in Flash, HSI (24 MHz) as system clock FLS_SLPTIME [1:0] = 00	10.2	-	μs
			Run program in Flash, HSI (48 MHz) as system clock FLS_SLPTIME [1:0] = 00	9.8		
$t_{WUDEEPSTOP}$	Wake-up from Deep_stop mode	DLP	Run program in Flash, HSI (24 / 48 MHz) as system clock FLS_SLPTIME [1:0] = 00	380	-	μs
$t_{WUHIBERNATE}$	Wake-up from Hibernate mode	HIB	Run program in Flash, HSI (24 / 48 MHz) as system clock FLS_SLPTIME [1:0] = 00	380	-	μs

1. The wake-up time is measured from the wake-up time until the first instruction is read by the user program.
2. Data based on characterization results, not tested in production.

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5.3.6. External clock source characteristics

5.3.6.1. High-speed external clock generated from an external source

In HSE bypass mode (HSEON of RCC_CR is set), the corresponding IO acts as an external clock input port.

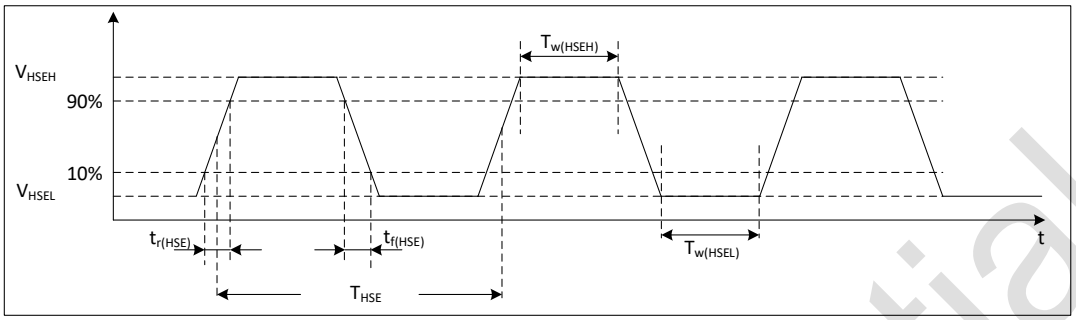

Figure 5-2 High-speed external clock timing diagram

Table 5-13 High-speed external clock characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	1	8	32	MHz
V_{HSEH}	Input pin high level voltage	0.7*V_{CC}	-	V_{CC}	V
V_{HSEL}	Input pin low level voltage	V_{SS}	-	0.3*V_{CC}	V
$t_{W(HSEH)}$ $t_{W(HSEL)}$	High or low time	15(1)	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	Rise or fall time	-	-	20(1)	ns

1. Guaranteed by design, not tested in production.

5.3.6.2. Low-speed external clock generated from an external source

In the bypass mode of LSE (the LSEBYP of RCC_BDCR is set), the low-speed start-up circuit in the device stops working, and the corresponding I/O is used as a standard GPIO.

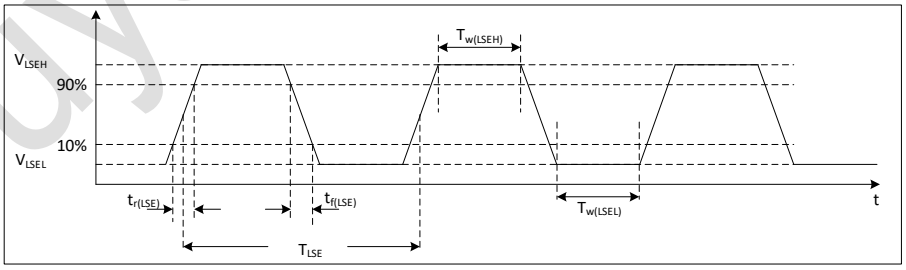

Figure 5-3 Low-speed external clock timing diagram

Table 5-14 Low-speed external clock characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	32.768	1000	kHz
V_{LSEH}	Input pin high level voltage	0.7*V_{CC}	-	-	V

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Symbol	Parameter	Min	Typ	Max	Unit
V_{LSEL}	Input pin low level voltage	-	-	0.3*V_{CC}	V
$t_{W(LSEH)}$ $t_{W(LSEL)}$	High or low time	450(1)	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	Rise or fall time	-	-	50(1)	ns

1. Guaranteed by design, not tested in production.

5.3.6.3. High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with 4 - 8 MHz crystal/ceramic resonator oscillator. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time.

Table 5-15 HSE oscillator characteristics(1)

Symbol	Parameter	Conditions	Min(2)	Typ	Max(2)	Unit
f_{OSC_IN}	Oscillator frequency	-	4	-	8	MHz
I_{CC}(4)	HSE current consumption	Startup time	-	-	5.5	mA
		V_{CC}=3 V, Rm=35 Ω, C_L=15 pF@8 MHz HSE_DRV = 1	-	0.7	-	
		V_{CC}=3 V, Rm=35 Ω, C_L=15 pF@4 MHz HSE_DRV = 0	-	0.6	-	
$t_{SU(HSE)}$(3) (4)	Startup time	f_{OSC_IN}= 8 MHz Rm=35 Ω, C_L=15 pF@8 MHz LSE_STARTUP [1:0] = 00 HSE_DRV = 1	-	2.5	-	ms
		f_{OSC_IN}= 4 MHz Rm=35 Ω, C_L=15 pF@4 MHz LSE_STARTUP [1:0] = 00 HSE_DRV = 1	-	4.0	-	
		f_{OSC_IN}= 4 MHz Rm=35 Ω, C_L=15 pF@4 MHz LSE_STARTUP [1:0] = 00 HSE_DRV = 0	-	5.0	-	

1. Crystal/ceramic resonator characteristics are based on the manufacturer's datasheet.
2. Guaranteed by design, not tested in production.
3. $t_{SU(HSE)}$ is the startup time from enable (by software) to when the clock oscillation reaches a stable state, measured for a standard crystal/resonator, which can vary considerably from one crystal/resonator to another.
4. Data based on characterization results, not tested in production.

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5.3.6.4. Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time.

Table 5-16 LSE oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}(3)	LSE current consumption	LSE_DRIVER [1:0] = 00	-	400	-	nA
		LSE_DRIVER [1:0] = 01	-	500	-	
		LSE_DRIVER [1:0] = 10	-	700	-	
		LSE_DRIVER [1:0] = 11	-	1200	-	
$t_{SU(LSE)}$(2)(3)	Startup time	f_{OSC_IN}= 32.768 kHz, C_L=6 pF LSE_STARTUP [1:0] = 00 LSE_DRIVER [1:0] = 00	-	2.60	-	s
		f_{OSC_IN}= 32.768 kHz, C_L=6 pF LSE_STARTUP [1:0] = 00 LSE_DRIVER [1:0] = 01	-	1.20	-	
		f_{OSC_IN}= 32.768 kHz, C_L=12 pF LSE_STARTUP [1:0] = 00 LSE_DRIVER [1:0] = 10	-	0.85	-	
		f_{OSC_IN}= 32.768 kHz, C_L=12 pF LSE_STARTUP [1:0] = 00 LSE_DRIVER [1:0] = 11	-	0.50	-	

1. Crystal/ceramic resonator characteristics are based on the manufacturer's datasheet.
2. $t_{SU(LSE)}$ is the startup time from enable (by software) to when the clock oscillation reaches a stable, measured for a standard crystal/resonator, which may vary greatly from crystal to resonator.
3. Data based on characterization results, not tested in production.

5.3.7. High-speed internal (HSI) RC oscillator

Table 5-17 HSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	HSI frequency	T_A = 25 °C, V_{CC} = 3.3 V	23.83(2)	24	24.17(2)	MHz
			47.66(2)	48	48.34(2)	
$ACC_{(HSI)}$	HSI accuracy	V_{CC} = 2.0 - 5.5 V T_A = -40 - 105 °C	-2(2)	-	2(2)	%
		V_{CC} = 1.8 - 5.5 V T_A = 0 - 105 °C	-2(2)	-	2(2)	
		V_{CC} = 1.8 - 5.5 V T_A = -40 - 105 °C	-3(2)	-	3(2)	
f_{TRIM}(1)	HSI trimming accuracy	-	-	0.1	-	%
D_{HSI}(1)	Duty cycle	-	45	-	55	%

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{Stab(HSI)}$	HSI stabilization time	-	-	2	4(1)	μs
$I_{CC(HSI)}$ (2)	HSI power consumption	48 MHz		300		μA
		24 MHz	-	220	-	

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

5.3.8. Low-speed internal (LSI) RC oscillator

Table 5-18 HSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI frequency	T_A = 25 °C, V_{CC} = 3.3 V	31.6	32.768	33.6	kHz
$ACC_{(LSI)}$	LSI accuracy	V_{CC} = 1.8 - 5.5 V T_A = 0 - 105 °C	-8(2)	-	8(2)	%
		V_{CC} = 1.8 - 5.5 V T_A = - 40 - 105 ℃	-10(2)	-	10(2)	
f_{TRIM}(1)	LSI trimming accuracy	-	-	0.2	-	%
$t_{Stab(LSI)}$ (1)	LSI stabilization time	-	-	150	-	μs
$I_{CC(LSI)}$ (1)	LSI power consumption	-	-	210	-	nA

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

5.3.9. Memory characteristics

Table 5-19 Memory characteristics

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
t_{prog}	Page programming time	-	1.5	2.0	ms
t_{ERASE}	Page/sector/mass erase time	-	3.5	4.5	ms
I_{CC}	Page programming supply current	-	2.1	2.9	mA
	Page/sector/mass erase supply current	-	2.1	2.9	

1. Guaranteed by design, not tested in production.

Table 5-20 Memory endurance and data retention

Symbol	Parameter	Conditions	Min(1)	Unit
N_{END}	Endurance	T_A = -40 - 85 °C	100	kcycle
		T_A = 85 - 105 °C	10	
t_{RET}	Data retention time	10 kcycle T_A = 55 °C	20	Year

1. Data based on characterization results, not tested in production.

5.3.10. EFT characteristics

Table 5-21 EFT characteristics

Symbol	Parameter	Conditions	Grade
EFT to Power	-	IEC61000-4-4	4A

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5.3.11. ESD & LU characteristics

Table 5-22 ESD & LU characteristics

Symbol	Parameter	Conditions	Typ	Unit
$V_{ESD(HBM)}$	Static discharge voltage (human body model)	ESDA/JEDEC JS-001-2017	8	kV
$V_{ESD(CDM)}$	Static discharge voltage (charged device model)	ESDA/JEDEC JS-002-2018	2	kV
LU	Static Latch-up	JESD78E	200	mA

5.3.12. Port characteristics

Table 5-23 Port static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	Input high level voltage	V_{CC} = 1.8 - 5.5 V	0.7*V_{CC}	-	-	V
V_{IL}	Input low level voltage	V_{CC} = 1.8 - 5.5 V	-	-	0.3*V_{CC}	V
V_{hys}(1)	Schmitt trigger hysteresis	-	-	150	-	mV
I_{lkg}	Input leakage current	-	-	-	1	μA
R_{PU}	Weak pull-up equivalent resistor	V_{IN} = V_{SS}, IORP<1:0>=11	24	40	56	kΩ
		V_{IN} = V_{SS}, IORP<1:0>=10	12	20	28	
		V_{IN} = V_{SS}, IORP<1:0>=01	6.6	11	15.4	
		V_{IN} = V_{SS}, IORP<1:0>=00	-	OFF	-	
R_{PD}	Weak pull-down equivalent resistor	V_{IN} = V_{SS}, IORP<1:0>=11	24	40	56	kΩ
		V_{IN} = V_{SS}, IORP<1:0>=10	12	20	28	
		V_{IN} = V_{SS}, IORP<1:0>=01	6.6	11	15.4	
		V_{IN} = V_{SS}, IORP<1:0>=00	-	OFF	-	
R_{PUIIC}	I^2C pull-up resistor	PU=0, PU_IIC=1	3.4	4.7	6.0	kΩ
C_{IO}(1)	Pin capacitance	-	-	5	-	pF
$t_{ns(EXTI)}$(1)	Input filter width	ENI=1, ENS=1	3	5	10	ns

1. Guaranteed by design, not tested in production.

Table 5-24 Output voltage characteristics(1)

Symbol	Parameter(4)	Conditions(2)	Min	Max	Unit
V_{OL}(3)	COM and COM_P IO output low level	I_{OL} = 20 mA, V_{CC} ≥ 5.0 V	-	0.6	V
		I_{OL} = 8 mA, V_{CC} ≥ 2.7 V	-	0.4	
		I_{OL} = 4 mA, V_{CC} = 1.8 V	-	0.4	
	COM_L output low level	I_{OL} = 80 mA, V_{CC} ≥ 3.3 V	-	0.6	V
		I_{OL} = 60 mA, V_{CC} ≥ 2.7 V	-	0.6	
		I_{OL} = 40 mA, V_{CC} ≥ 1.8 V	-	0.6	
V_{OH}(3)	COM and COM_L IO output high level	I_{OH} = 20 mA, V_{CC} ≥ 5.0 V	V_{CC}–0.6	-	V
		I_{OH} = 8 mA, V_{CC} ≥ 2.7 V	V_{CC}–0.4	-	
		I_{OH} = 4 mA, V_{CC} = 1.8 V	V_{CC}–0.5	-	
	COM_P IO output high level	I_{OH} = 30 mA, V_{CC} ≥ 5.0 V	V_{CC}–0.6	-	

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Symbol	Parameter[4]	Conditions[2]	Min	Max	Unit
		I_{OH} = 20 mA, V_{CC} ≥ 2.7 V	V_{CC}–0.6	-	
		I_{OH} = 4 mA, V_{CC} = 1.8 V	V_{CC}–0.5	-	

1. The combined maximum current across all output pins (including contributions from both V_{OL} and V_{OH} states) must not exceed the $\Sigma I_{IO(PIN)}$ maximum rating specified in Table 5-2 Current Characteristics.
2. The test conditions for driving all IOs is that GPIOx_OSPEEDR = 11.
3. These I/O types refer to the terms and symbols defined by pins.
4. Data based on characterization results, not tested in production.

5.3.13. ADC characteristics

Table 5-25 ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	ADC supply voltage for ADC ON	-	1.8	-	5.5	V
I_{CC}[1]	Consumption	f_s =0.75 Msps	-	1	-	mA
C_{IN}[1]	Internal sampling and holding capacitor	-	-	5	-	pF
f_{ADC}	ADC clock frequency	V_{REF+} =V_{CC}=1.8 - 2.3 V	0.8	4	8[2]	MHz
		V_{REF+} =V_{CC}=2.3 - 5.5 V	0.8	8	12[2]	
		V_{REF+} = V_{REFBUF}, V_{CC}=1.8 - 2.3 V	0.16	0.8	1.6[2]	
		V_{REF+} = V_{REFBUF}, V_{CC}=2.3 - 5.5 V	0.16	1.6	2.4[2]	
t_{samp}[1]	Sampling time	V_{CC}=1.8 - 5.5 V	3.5	-	239.5	1/f_{ADC}
t_{samp_setup}[1]	Sampling time for internal channels (V_{REFINT}, V_{CC}/3)	-	20	-	-	μs
t_{conv}[1]	Total conversion time	-	-	12	-	1/f_{ADC}
t_{eoc}[1]	Conversion end time	-	-	0.5	-	1/f_{ADC}

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

Table 5-26 ADC accuracy (V_{REF+} = V_{CC})

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ET	Total unadjusted error	V_{CC} = 3.3 V, T_A = 25 °C f_{ADC} = 12 MHz , f_s = 0.75 Msps	-	±4	±7	LSB
EO	Offset error		-4	-2.5	-	
EG	Gain error		-	8.5	10.5	
ED	Differential linearity error		-	+3 -0.9	+4 -1	
EL	Integral linearity		-	±3.5	±4.5	
ENOB	Effective number of bits		8.9	9.5	-	bit
ET	Total unadjusted error	1.8 V ≤ V_{CC} ≤ 5.5 V	-	±4	±10.5	LSB

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
EO	Offset error	f_{ADC} ≤ 12 MHz , f_s ≤ 0.75 Msps	-5	-2.5	-	
EG	Gain error		-	8.5	13	
ED	Differential linearity error		-	+3 -0.9	+5 -1	
EL	Integral linearity		-	±3.5	±6	
ENOB	Effective number of bits		8.8	9.5	-	bit

Table 5-27 ADC accuracy (V_{REF+} = V_{CC})

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ET	Total unadjusted error	V_{REFBUF} = 1.5 V/2.048 V/2.5 V V_{CC} = 3.3 V, T_A = 25 °C f_{ADC} = 12 MHz , f_s = 0.15 Msps	-	±6	±9	LSB
EO	Offset error		-7	-4	-	
EG	Gain error		-	8	11.5	
ED	Differential linearity error		-	+3.5 -0.9	+4.5 -0.95	
EL	Integral linearity		-	±4.5	±5	
ENOB	Effective number of bits		8.5	8.8	-	bit
ET	Total unadjusted error	V_{REFBUF} = 1.5 V/2.048 V/2.5 V V_{CC} = 3.3 V, T_A = 25 °C f_{ADC} = 12 MHz , f_s = 0.15 Msps	-	±16.5	±24.5	LSB
EO	Offset error		-16	-11	-	
EG	Gain error		-	13	18	
ED	Differential linearity error		-	+5.5 -0.9	+9 -0.95	
EL	Integral Linearity		-	±14	±16	
ENOB	Effective number of bits		7.2	7.3	-	bit
ET	Total unadjusted error	V_{REFBUF} =1.5 V, 1.8 V ≤ V_{CC} ≤ 5.5 V V_{REFBUF} 2.048 V, 2.4 V ≤ V_{CC} ≤ 5.5 V V_{REFBUF} 2.5 V, 2.8 V ≤ V_{CC} ≤ 5.5 V f_{ADC} ⩽ 2.4 MHz , f_s ⩽ 0.15 Msps	-	±6	±13	LSB
EO	Offset error		-11	-4	-	
EG	Gain error		-	8	-	
ED	Differential linearity error		-	+3.5 -0.9	+6.5 -1	
EL	Integral linearity		-	±4.5	±7.5	
ENOB	Effective number of bits		8.5	8.8	-	bit
ET	Total unadjusted error	V_{REFBUF} 0.6 V, 1.8 V ≤ V_{CC} ≤ 5.5 V f_{ADC} = 12 MHz , f_s ⩽ 0.15 Msps	-	±16.5	±30	LSB
EO	Offset error		- 20.5	-11	-	
EG	Gain error		-	13	-	
ED	Differential linearity error		-	+5.5	+11.5	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
				-0.9	-1	
EL	Integral linearity		-	±14	±17	
ENOB	Effective number of bits		7.2	7.3	-	bit

5.3.14. Comparator characteristics

Table 5-28 Comparator characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IN}	Input voltage range	-		0	-	V_{CC}-1.5	V
t_{START}(1)	Startup time	High-speed mode		-	-	5	µs
		Medium-speed mode		-	-	15	
t_D (1)	Propagation delay	High-speed mode	200 mV step 100 mV over-drive	-	0.2	-	µs
		Medium-speed mode		-	-	1.2	
		High-speed mode	>200 mV step 100 mV over-drive	-	0.2	-	
		Medium-speed mode		-	-	1.2	
V_{offset}(1)	Offset voltage	-		-	±5	-	mV
I_{CC}(1)	Comsumption	High-speed mode	Static	-	70	-	µA
			With 50 kHz and ± 100 mv overdrive square signal	-	70	-	
		Medium-speed mode	Static	-	6	7.5	
			With 50 kHz and ± 100 mv overdrive square signal	-	5	-	
I_{sleep} (1)	Sleep power consumption	-	-	-	1	-	nA

1. Guaranteed by design, not tested in production.

5.3.15. Temperature sensor characteristics

Table 5-29 Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{TS} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	2	2.6	3.2	mV/°C
V_{30}	Voltage at 30 ℃ (±5 ℃)	742	760	785	mV
t_{samp_setup}(1)	ADC sampling time when reading the temperature	20	-	-	µs

1. Guaranteed by design, not tested in production.

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5.3.16. Embedded voltage reference characteristics

Table 5-30 Embedded internal voltage reference (V_{REFINT}) characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	1.17	1.20	1.23	V
$t_{start\_VREFINT}$	Start time of V_{REFINT}	-	10	15	μs
$T_{coeff\_VREFINT}$(1)	Temperature coefficient of V_{REFINT}	-	-	100(1)	ppm/°C
I_{vcc}(1)	Current consumption from V_{CC}	-	12	20	μA

1. Guaranteed by design, not tested in production.

5.3.17. ADC voltage reference buffer characteristics

Table 5-31 Embedded internal voltage reference (V_{REFBUF}) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REF25}	2.5 V Internal reference voltage	T_A = 25 °C，V_{CC} = 3.3 V	2.475	2.5	2.525	V
V_{REF20}	2.048 V Internal reference voltage	T_A = 25 °C，V_{CC} = 3.3 V	2.028	2.048	2.068	V
V_{REF15}	1.5 V Internal reference voltage	T_A = 25 °C，V_{CC} = 3.3 V	1.485	1.5	1.515	V
V_{REF06}	0.6 V Internal reference voltage	T_A = 25 °C，V_{CC} = 3.3 V	0.594	0.6	0.606	V
$T_{coeff\_VREFINT}$(1)	Temperature coefficient of V_{REFBUF}	T_A = -40 - 105 °C	-	-	120	ppm/°C
			-	-	300(2)	
$t_{start\_VREFBUF}$	Start time of V_{REFBUF}	-	-	10	15	μs

1. Guaranteed by design, not tested in production.
2. V_{REFBUF}= 0.6 V.

5.3.18. COMP internal reference voltage characteristics

Table 5-32 Embedded internal voltage reference (V_{REFCMP}) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ΔV_{abs} (1)	Absolute deviation	-	-	-	±0.5	LSB
$t_{start\_VREFCMP}$	Start time of V_{REFCMP}	-	-	10	15	μs

5.3.19. Timer characteristics

Table 5-33 Timer characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	20.833	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	-	$f_{TIMxCLK}$/2	MHz
		$f_{TIMxCLK}$ = 48 MHz	-	24	
Res_{TIM}	Timer resolution time	TIM1/14	-	16	bit
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	0.020833	1365	μs

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Table 5-34 IWDG characteristics (timeout period at 32.768 kHz LSI)

Prescaler	PR[2:0]	Min	Max	Unit
/4	0	0.122	499.712	ms
/8	1	0.244	999.424	
/16	2	0.488	1998.848	
/32	3	0.976	3997.696	
/64	4	1.952	7995.392	
/128	5	3.904	15990.784	
/256	6 or 7	7.808	31981.568	

5.3.20. Communication interfaces

5.3.20.1. I²C interface characteristics

I²C interface meets the requirements of the I²C bus specification and user manual:

- Standard-mode (Sm): 100 kHz
- Fast-mode (Fm): 400 kHz
- Fast-mode plus (Fm+): 1 MHz

I²C SDA and SCL pins have analog filtering, see table below.

Table 5-35 I²C filter characteristics

Symbol	Parameter	Min	Max	Unit
t_{AF}	Limiting duration of spikes suppressed by the filter (spikers shorter than the limiting duration are suppressed)	50	260	ns

5.3.20.2. SPI characteristics

Table 5-36 SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	24(1)	MHz
		Slave mode	-	24(2)	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 15 pF	-	6	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	2 T_{pclk}	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	2 T_{pclk}	-	ns
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Slave mode, presc = 2	T_{pclk} - 2	T_{pclk} + 1	ns
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode	1	-	ns
		Slave mode	3	-	
$t_{h(MI)}$ $t_{h(SI)}$	Data input hold time	Master mode	5	-	ns
		Slave mode	2	-	
$t_{a(SO)}$	Data output access time	Slave mode	0	3 T_{pclk}	ns
$t_{dis(SO)}$	Data output access time	Slave mode	2 T_{pclk}	-	ns
$t_{v(SO)}$	Data output valid time	Slave mode (after enable edge)	0	20	ns

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Symbol	Parameter	Conditions	Min	Max	Unit
$t_{v(MO)}$	Data output valid time	Master mode (after enable edge)	-	5	ns
$t_{h(SO)}$	Data output hold time	Slave mode (after enable edge)	2	-	ns
$t_{h(MO)}$		Master mode (after enable edge)	1	-	
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	45	55	%

1. The test condition for this parameter is full-duplex mode.
2. Under full-duplex mode, the maximum is 6 MHz, while under single-wire (transmit-only) mode, the maximum is 12 MHz.

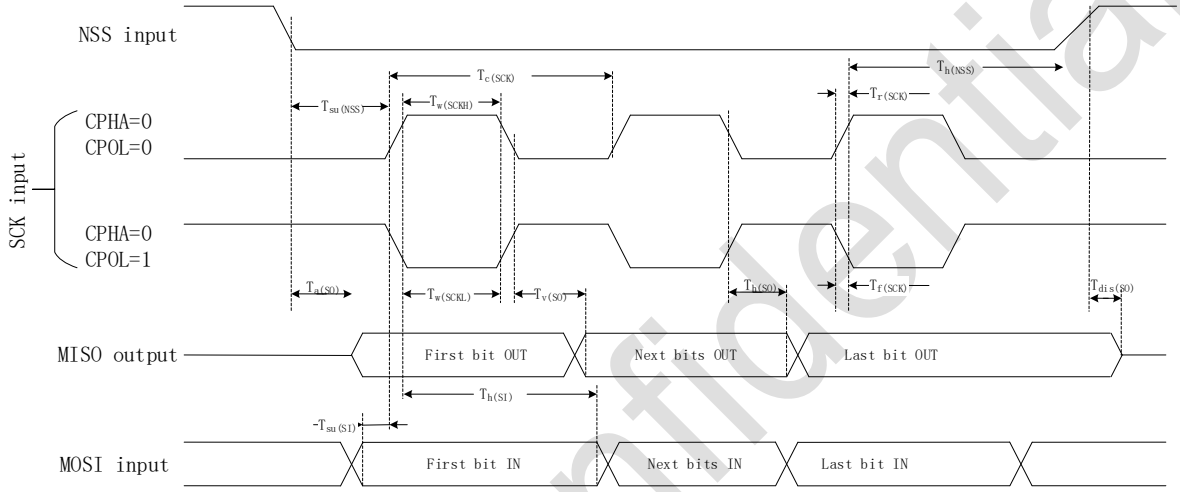

Figure 5-4 SPI timing diagram–Slave mode and CPHA=0

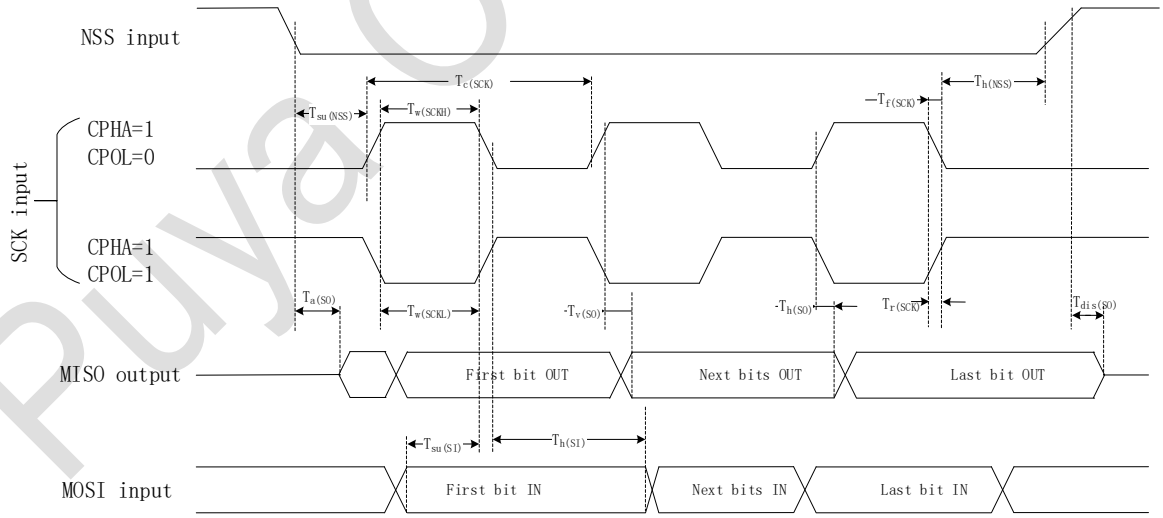

Figure 5-5 SPI timing diagram–Slave mode and CPHA=1

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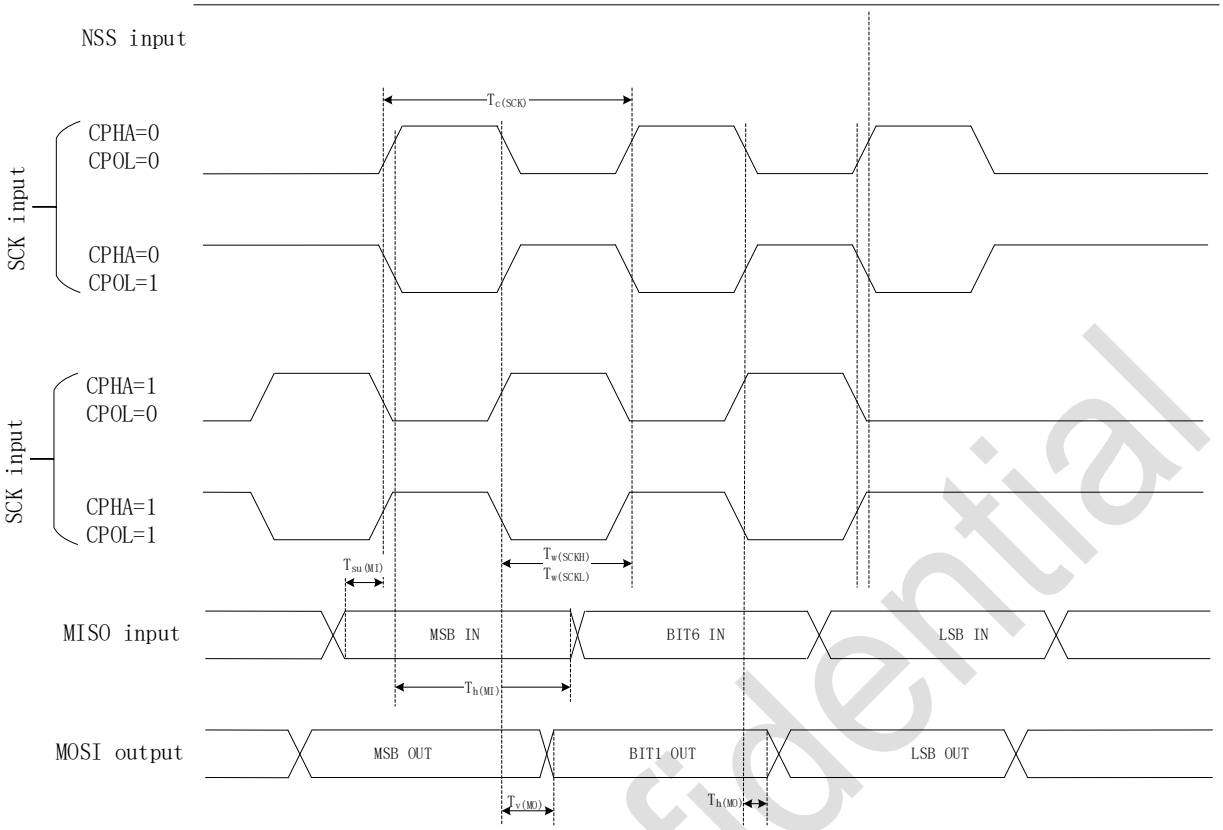

Figure 5-6 SPI timing diagram–Master mode

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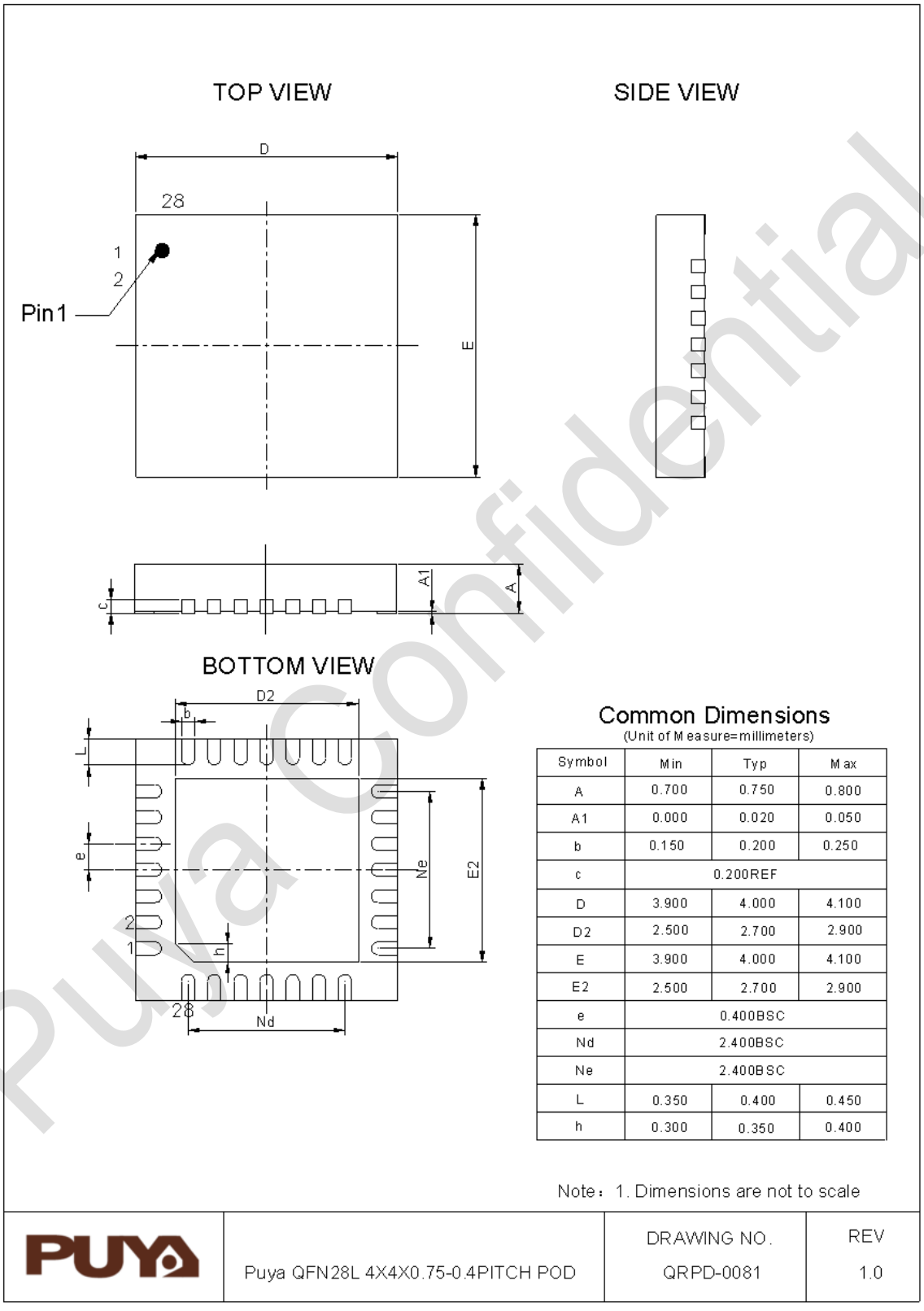
6. Package information

6.1. QFN28 package size



Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	0.700	0.750	0.800
A1	0.000	0.020	0.050
b	0.150	0.200	0.250
c		0.200REF	
D	3.900	4.000	4.100
D2	2.500	2.700	2.900
E	3.900	4.000	4.100
E2	2.500	2.700	2.900
e		0.400BSC	
Nd		2.400BSC	
Ne		2.400BSC	
L	0.350	0.400	0.450
h	0.300	0.350	0.400

Note：1. Dimensions are not to scale

PUYA	Puya QFN28L 4X4X0.75-0.4PITCH POD	DRAWING NO. QRPD-0081	REV 1.0

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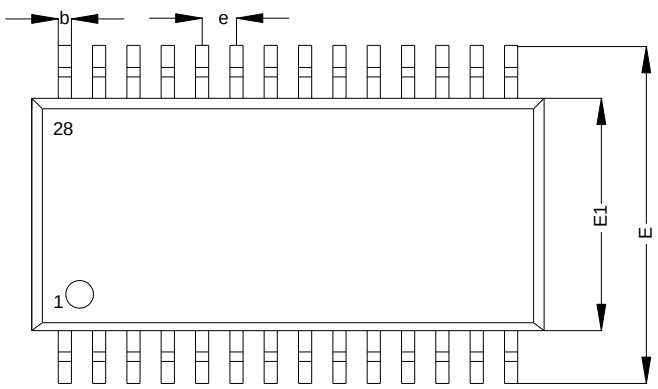
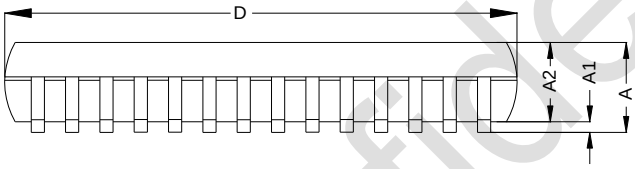
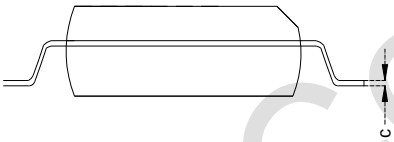
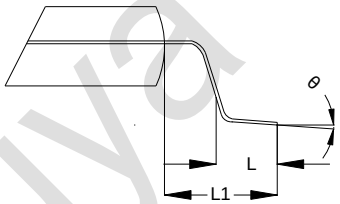
6.2. TSSOP28 package size









Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	0.85	-	1.20
A1	0.05	-	0.15
A2	0.80	1.00	1.05
b	0.19	-	0.30
c	0.14	-	0.18
D	9.60	9.70	9.80
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0	-	8°

Note: Dimensions are not to scale.

	TITLE	DRAWING NO.	REV
PUYA	PUYA TSSOP28 POD	QRPD-0073	1.0

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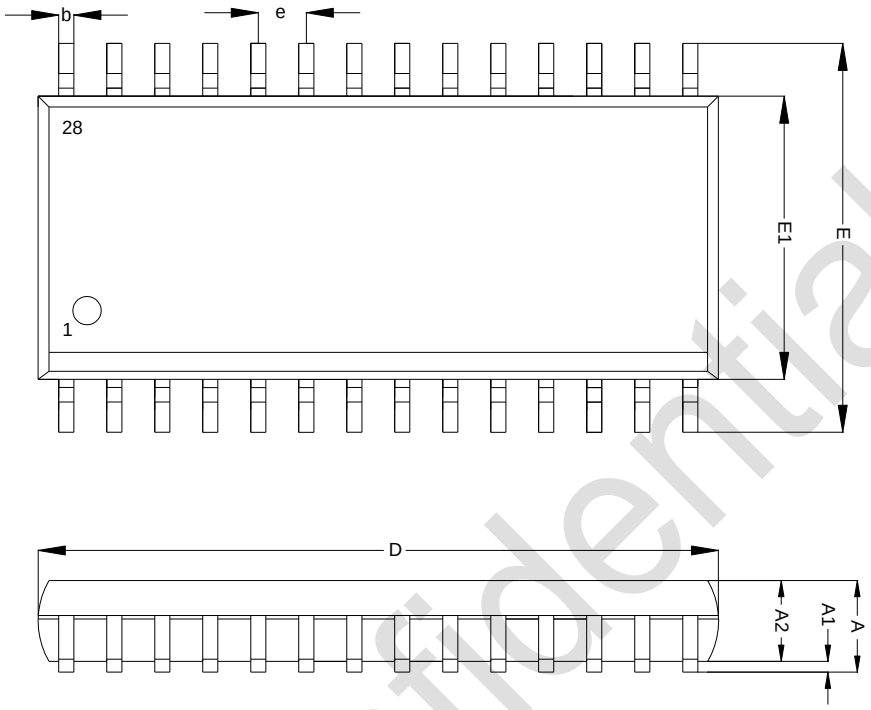
6.3. SOP28 package size



Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	2.15	-	2.65
A1	0.10	-	0.30
A2	2.05	-	2.35
b	0.38	-	0.48
c	0.24	-	0.30
D	17.80	18.00	18.20
E	10.10	10.30	10.50
E1	7.30	7.50	7.70
e	1.27BSC		
L	0.60	-	1.00
L1	1.40REF		
θ	0	-	8°

Note: Dimensions are not to scale.

	TITLE	DRAWING NO.	REV
PUYA	PUYA SOP28 (300mil) POD	QRPD-0072	1.0

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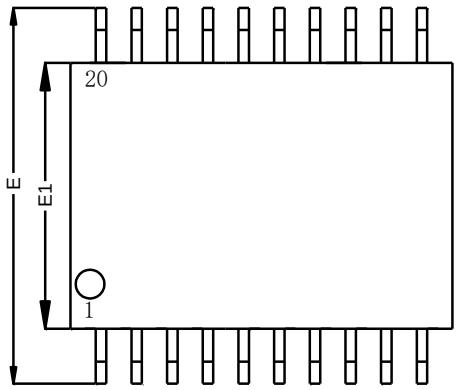
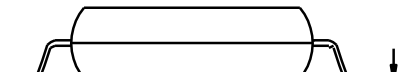
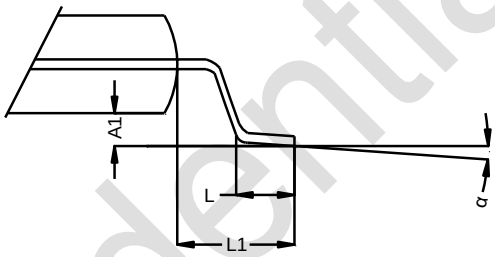
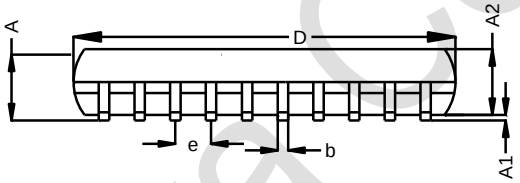
6.4. SOP20 package size









Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	-	-	2.650
A1	0.100	-	0.300
A2	2.100	2.300	2.500
b	0.330	-	0.510
c	0.200	-	0.330
D	12.600	12.800	13.000
E	10.100	10.300	10.500
E1	7.400	7.500	7.600
e	1.275BSC		
h	0.300	-	0.500
L	0.400	-	1.270
L1		1.400REF	
θ	0	-	8°

Note：1. Dimensions are not to scale

	TITLE	DRAWING NO.	REV
PUYA	Puya SOP20 POD	QRPD-0048	1.0

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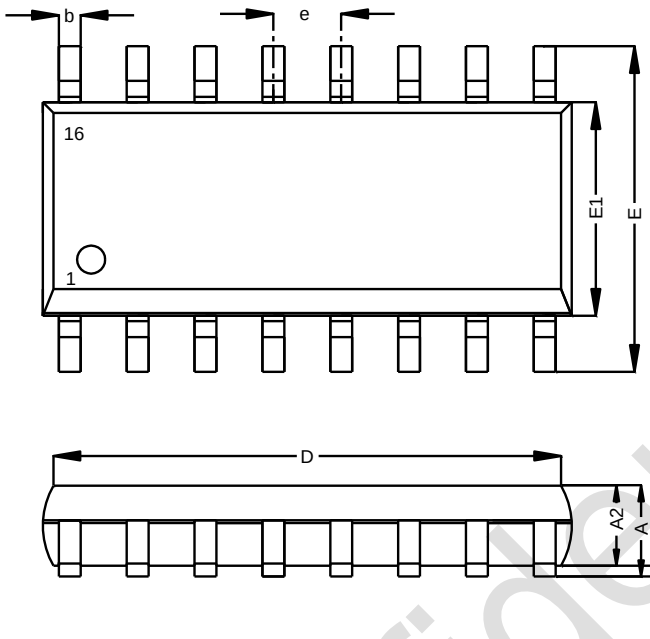
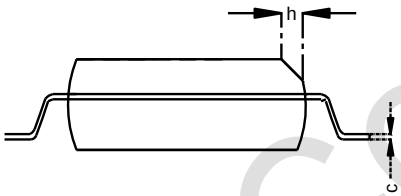
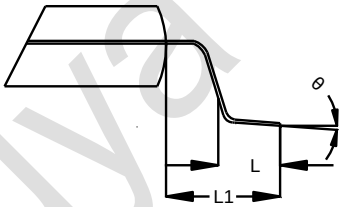
6.5. SOP16 package size







Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	-	-	1.75
A1	0.10	-	0.25
A2	1.30	-	-
b	0.31	-	0.51
c	0.10	-	0.25
D	9.80	-	10.20
E	5.80	-	6.20
E1	3.80	-	4.20
e	1.27BSC		
L	0.40	-	1.27
L1	1.05REF		
θ	0	-	8°
h	0.25	-	0.50

Note: Dimensions are not to scale.

	TITLE	DRAWING NO.	REV
PUYA	PUYA SOP16 (150mil) POD	QRPD-0001	1.1

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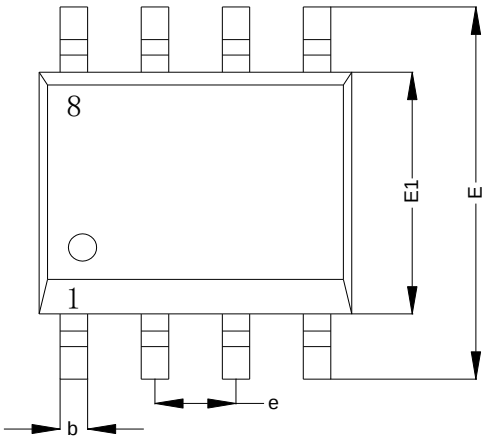
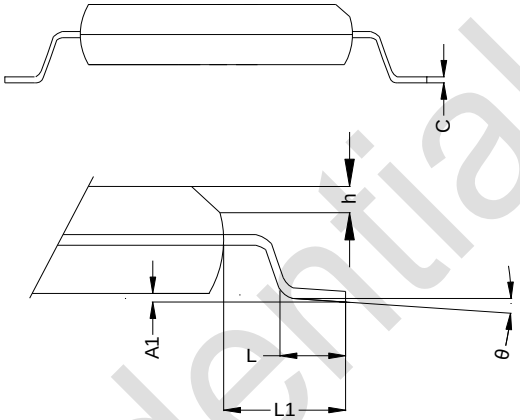
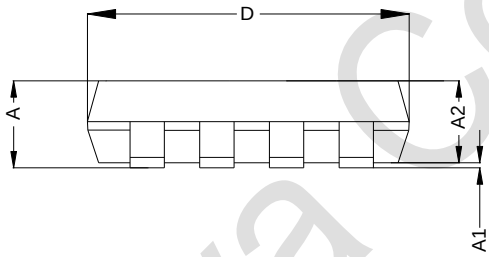
6.6. SOP8 package size







Common Dimensions

(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	1.350	-	1.750
A1	0.100	-	0.250
A2	1.250	-	-
b	0.310	-	0.510
c	0.170	-	0.250
D	4.800	4.900	5.000
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
e	-	1.270	-
L	0.400	-	1.270
L1	-	1.050	-
θ	0	-	8°
h	0.25	-	0.50

Note：1. Dimensions are not to scale

	TITLE	DRAWING NO.	REV
PUYA	Puya SOP8（150mil）POD	QRPD-0004	1.1

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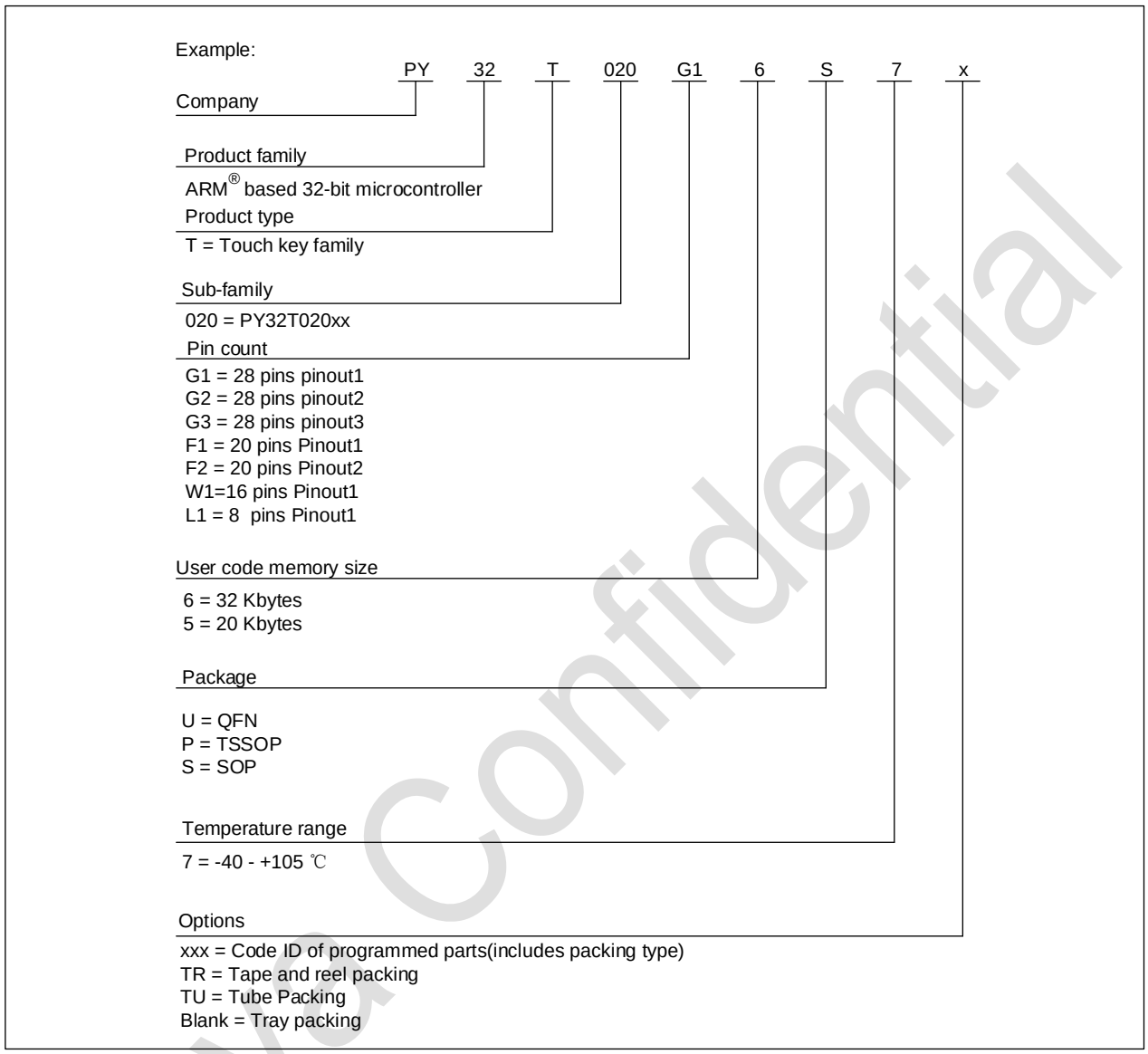
7. Ordering information



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8. Version history

Version	Date	Description
V1.0	2025.04.03	Initial version
V1.1	2025.04.03	Consistent with the Chinese version No.

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